

INSTRUCTION EXECUTION TIMES



In This Appendix:

Introduction	C-2
Instruction Execution Times	C-3

Introduction

This appendix contains several tables that provide the instruction execution times for DL05 Micro PLCs. Many of the execution times depend on the type of data used with the instruction. Registers may be classified into the following types:

- Data (word) Registers
- Bit Registers

V-memory Data Registers

Some V-memory locations are considered data registers, such as timer or counter current values. Standard user V-memory is classified as a V-memory data register. Note that you can load a bit pattern into these types of registers, even though their primary use is for data registers. The following locations are data registers:

Data Registers	DL05
Timer Current Values	V0 - V177
Counter Current Values	V1000 - V1177
User Data Words	V1200 - V7377 V7400 - V7577

V-memory Bit Registers

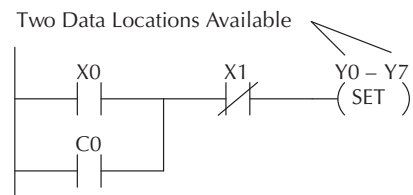
You may recall that some of the discrete points such as X, Y, C, etc. are automatically mapped into V-memory. The following bit registers contain this data:

How to Read the Tables

Bit Registers	DL05
Input Points (X)	V40400 - V40417
Output Points (Y)	V40500 - V40517
Control Relays (C)	V40600 - V40637
Stages (S)	V41000 - V41017
Timer status Bits	V41100 - V41107
Counter status Bits	V41140 - V41147
Special Relays (SP)	V41200 - V41237

Some instructions can have more than one parameter. For example, the SET instruction shown in the ladder program to the right can set a single point or a range of points.

In these cases, execution times depend on the amount and type of parameters. The execution time tables list execution times for both situations, as shown below:



SET	1st #: X, Y, C, 2nd #: X, Y, C, S (N pt)	9.2 μ s 9.6 μ s + 0.9 V x N
RST	1st #: X, Y, C, 2nd #: X, Y, C, S (N pt)	9.2 μ s 9.6 μ s + 0.9 V x N

Execution depends on numbers of locations and types of data used

Instruction Execution Times

Boolean Instructions

Boolean Instructions		DL05	
Instruction	Legal Data Types	Execute	Not Execute
STR	X, Y, C, T, CT, S, SP	2.0 μs	2.0 μs
STRN	X, Y, C, T, CT, S, SP	2.2 μs	2.2 μs
OR	X, Y, C, T, CT, S, SP	2.5 μs	2.4 μs
ORN	X, Y, C, T, CT, S, SP	2.5 μs	2.4 μs
AND	X, Y, C, T, CT, S, SP	2.2 μs	2.1 μs
ANDN	X, Y, C, T, CT, S, SP	2.3 μs	2.3 μs
ANDSTR	None	1.2 μs	1.2 μs
ORSTR	None	1.2 μs	1.2 μs
OUT	X, Y, C	6.8 μs	7.0 μs
OROUT	X, Y, C	6.7 μs	7.2 μs
NOT	None	1.6 μs	1.6 μs
PD	X, Y, C	55.0 μs	55.0 μs
STRPD	X, Y, C, T, CT, S, SP	20.2 μs	12.9 μs
STRND	X, Y, C, T, CT, S, SP	20.1 μs	13.0 μs
ORPD	X, Y, C, T, CT, S, SP	20.0 μs	12.6 μs
ORND	X, Y, C, T, CT, S, SP	19.8 μs	12.7 μs
ANDPD	X, Y, C, T, CT, S, SP	20.0 μs	12.6 μs
ANDND	X, Y, C, T, CT, S, SP	19.9 μs	12.8 μs
SET	1st #: X, Y, C, S, 2nd #: X, Y, C, S (N pt)	42.0 μs 32.4 μs + 25.6 μs x N	3.7 μs 4.7 μs
RST	1st #: X, Y, C, S 2nd #: X, Y, C, S (N pt)	44.5 μs 33.8 μs + 25.7 μs x N	3.9 μs 4.8 μs
	1st #: T, CT 2nd #: T, CT (N pt)	73.0 μs 80.9 μs + 2.6 μs x N	3.7 μs 4.8 μs
PAUSE	1wd: Y 2wd: Y (N pt)	31.6 μs 48.4 μs + 12.1 μs x N	31.1 μs 48.8 μs



Comparative Boolean Instructions

Comparative Boolean Instructions		DL05		
Instruction	Legal Data Types		Execute	Not Execute
STRE	<i>1st</i> V: Data Reg.	<i>2nd</i> V:Data Reg.	16.5 μs	16.4 μs
		V:Bit Reg	16.5 μs	16.4 μs
	V: Bit Reg	K:Constant	11.9 μs	11.7 μs
		P:Indir. (Data)	62.9 μs	62.8 μs
		P:Indir. (Bit)	62.9 μs	62.8 μs
		V:Data Reg	16.5 μs	16.4 μs
		V:Bit Reg	16.5 μs	16.4 μs
		K:Constant	11.9 μs	11.7 μs
	P: Indir. (Data)	P:Indir. (Data)	62.9 μs	62.8 μs
		P:Indir. (Bit)	62.9 μs	62.8 μs
		V:Data Reg	63.1 μs	63.0 μs
		V:Bit Reg	63.1 μs	63.0 μs
	P: Indir. (Bit)	K:Constant	57.2 μs	57.1 μs
		P:Indir. (Data)	106.8 μs	106.6 μs
P:Indir. (Bit)		106.8 μs	106.6 μs	
V:Data Reg		63.1 μs	63.0 μs	
V:Bit Reg		63.1 μs	63.0 μs	
K:Constant		57.2 μs	57.1 μs	
STRNE	<i>1st</i> V: Data Reg	<i>2nd</i> V:Data Reg	16.6 μs	16.7 μs
		V:Bit Reg	16.6 μs	16.7 μs
	V: Bit Reg	K:Constant	12.0 μs	12.1 μs
		P:Indir. (Data)	63.0 μs	63.1 μs
		P:Indir. (Bit)	63.0 μs	63.1 μs
		V:Data Reg	16.6 μs	16.7 μs
		V:Bit Reg	16.6 μs	16.7 μs
		K:Constant	12.0 μs	12.1 μs
	P: Indir. (Data)	P:Indir. (Data)	63.0 μs	63.1 μs
		P:Indir. (Bit)	63.0 μs	63.1 μs
		V:Data Reg	63.3 μs	63.4 μs
		V:Bit Reg	63.3 μs	63.4 μs
	P: Indir. (Bit)	K:Constant	57.4 μs	57.5 μs
		P:Indir. (Data)	106.9 μs	107.0 μs
P:Indir. (Bit)		106.9 μs	107.0 μs	
V:Data Reg		63.3 μs	63.4 μs	
V:Bit Reg		63.3 μs	63.4 μs	
K:Constant		57.4 μs	57.5 μs	
	P:Indir. (Data)	106.9 μs	107.0 μs	
	P:Indir. (Bit)	106.9 μs	107.0 μs	

Comparative Boolean Instructions (cont'd)			DL05	
Instruction	Legal Data Types		Execute	Not Execute
ORE	1st V: Data Reg	2nd V:Data Reg	16.1 µs	16.0 µs
		V:Bit Reg	16.1 µs	16.0 µs
	V: Bit Reg	K:Constant	11.3 µs	11.2 µs
		P:Indir. (Data)	62.4 µs	62.2 µs
		P:Indir. (Bit)	62.4 µs	62.2 µs
		V:Data Reg.	16.1 µs	16.0 µs
		V:Bit Reg	16.1 µs	16.0 µs
		K:Constant	11.3 µs	11.2 µs
	P: Indir. (Data)	P:Indir. (Data)	62.4 µs	62.2 µs
		P:Indir. (Bit)	62.4 µs	62.2 µs
		V:Data Reg	62.6 µs	62.5 µs
		V:Bit Reg	62.6 µs	62.5 µs
	P: Indir. (Bit)	K:Constant	56.8 µs	56.8 µs
		P:Indir. (Data)	106.4 µs	106.2 µs
		P:Indir. (Bit)	106.4 µs	106.2 µs
		V:Data Reg	62.6 µs	62.5 µs
V:Bit Reg		62.6 µs	62.5 µs	
K:Constant		56.8 µs	56.8 µs	
ORNE	1st V: Data Reg.	2nd V:Data Reg.	16.3 µs	16.3 µs
		V:Bit Reg.	16.3 µs	16.3 µs
	V: Bit Reg.	K:Constant	11.5 µs	11.6 µs
		P:Indir. (Data)	62.5 µs	62.6 µs
		P:Indir. (Bit)	62.5 µs	62.6 µs
		V:Data Reg	16.3 µs	16.3 µs
		V:Bit Reg.	16.3 µs	16.3 µs
		K:Constant	11.5 µs	11.6 µs
	P: Indir. (Data)	P:Indir. (Data)	62.5 µs	62.6 µs
		P:Indir. (Bit)	62.5 µs	62.6 µs
		V:Data Reg.	62.7 µs	62.9 µs
		V:Bit Reg.	62.7 µs	62.9 µs
	P: Indir. (Bit)	K:Constant	57.0 µs	57.1 µs
		P:Indir. (Data)	106.5 µs	106.6 µs
		P:Indir. (Bit)	106.5 µs	106.6 µs
		V:Data Reg.	62.7 µs	62.9 µs
V:Bit Reg.		62.7 µs	62.9 µs	
K:Constant		57.0 µs	57.1 µs	
P: Indir. (Data)	P:Indir. (Data)	106.5 µs	106.6 µs	
	P:Indir. (Bit)	106.5 µs	106.6 µs	
	V:Data Reg.	62.7 µs	62.9 µs	
	V:Bit Reg.	62.7 µs	62.9 µs	
P: Indir. (Bit)	K:Constant	57.0 µs	57.1 µs	
	P:Indir. (Data)	106.5 µs	106.6 µs	
P: Indir. (Bit)	P:Indir. (Bit)	106.5 µs	106.6 µs	



Appendix C: Instruction Execution Times

Comparative Boolean Instructions (cont'd)			DL05	
Instruction	Legal Data Types		Execute	Not Execute
ANDE	<i>1st</i> V: Data Reg.	<i>2nd</i> V:Data Reg	16.1 μs	16.0 μs
		V:Bit Reg	16.1 μs	16.0 μs
	V: Bit Reg.	K:Constant	11.3 μs	11.3 μs
		P:Indir. (Data)	62.4 μs	62.2 μs
		P:Indir. (Bit)	62.4 μs	62.2 μs
		V:Data Reg	16.1 μs	16.0 μs
		V:Bit Reg	16.1 μs	16.0 μs
		K:Constant	11.3 μs	11.3 μs
	P: Indir. (Data)	P:Indir. (Data)	62.4 μs	62.2 μs
		P:Indir. (Bit)	62.4 μs	62.2 μs
		V:Data Reg	62.6 μs	62.5 μs
		V:Bit Reg	62.6 μs	62.5 μs
	P: Indir. (Bit)	K:Constant	56.9 μs	56.7 μs
		P:Indir. (Data)	106.4 μs	106.2 μs
		P:Indir. (Bit)	106.4 μs	106.2 μs
		V:Data Reg	62.6 μs	62.5 μs
V:Bit Reg		62.6 μs	62.5 μs	
K:Constant		56.9 μs	56.7 μs	
ANDNE	<i>1st</i> V: Data Reg.	<i>2nd</i> V:Data Reg.	16.2μs	16.4 μs
		V:Bit Reg.	16.2μs	16.4 μs
	V: Bit Reg.	K:Constant	11.5 μs	11.6 μs
		P:Indir. (Data)	62.5 μs	62.7 μs
		P:Indir. (Bit)	62.5 μs	62.7 μs
		V:Data Reg.	16.2 μs	16.4 μs
		V:Bit Reg	16.2 μs	16.4 μs
		K:Constant	11.5 μs	11.6 μs
	P: Indir. (Data)	P:Indir. (Data)	62.5 μs	62.7 μs
		P:Indir. (Bit)	62.5 μs	62.7 μs
		V:Data Reg.	62.7 μs	62.85 μs
		V:Bit Reg.	62.7 μs	62.85 μs
	P: Indir. (Bit)	K:Constant	57.0 μs	57.1 μs
		P:Indir. (Data)	106.5 μs	106.6 μs
		P:Indir. (Bit)	106.5 μs	106.6 μs
		V:Data Reg.	62.7 μs	62.85 μs
V:Bit Reg.		62.7 μs	62.85 μs	
K:Constant		57.0 μs	57.10 μs	
	P:Indir. (Data)	106.5 μs	106.6 μs	
	P:Indir. (Bit)	106.5 μs	106.6 μs	

Appendix C: Instruction Execution Times

Comparative Boolean Instructions (cont'd)			DL05		
Instruction	Legal Data Types		Execute	Not Execute	
STR	1st V: T, CT	2nd V:Data Reg.	16.5 µs	16.4 µs	
		V:Bit Reg.	16.5 µs	16.4 µs	
	V Data Reg	K:Constant	11.9 µs	11.7 µs	
		P:Indir. (Data)	62.9 µs	62.7 µs	
		P:Indir. (Bit)	62.9 µs	62.7 µs	
		V:Data Reg.	16.5 µs	16.4 µs	
		V:Bit Reg.	16.5 µs	16.4 µs	
		K:Constant	11.9 µs	11.7 µs	
	V: Bit Reg.	P:Indir. (Data)	62.9 µs	62.7 µs	
		P:Indir. (Bit)	62.9 µs	62.7 µs	
		V:Data Reg.	16.5 µs	16.4 µs	
		V:Bit Reg.	16.5 µs	16.4 µs	
		K:Constant	11.9 µs	11.7 µs	
		P:Indir. (Data)	62.9 µs	62.7 µs	
	P: Indir. (Data)	P:Indir. (Bit)	62.9 µs	62.7 µs	
		V:Data Reg.	63.1 µs	63.0 µs	
		V:Bit Reg.	63.1 µs	63.0 µs	
		K:Constant	56.2µs	57.1 µs	
		P:Indir. (Data)	106.8 µs	106.6 µs	
		P:Indir. (Bit)	106.8 µs	106.6 µs	
	STRN	1st V: T, CT	2nd V:Data Reg.	16.6 µs	16.7 µs
			V:Bit Reg.	16.6 µs	16.7 µs
		V: Data Reg.	K:Constant	12.0 µs	12.1 µs
			P:Indir. (Data)	63.0 µs	63.1 µs
P:Indir. (Bit)			63.0 µs	63.1 µs	
V:Data Reg.			16.6 µs	16.7 µs	
V:Bit Reg.			16.6 µs	16.7 µs	
K:Constant			12.0 µs	12.1 µs	
V: Bit Reg		P:Indir. (Data)	63.0 µs	63.1 µs	
		P:Indir. (Bit)	63.0 µs	63.1 µs	
		V:Data Reg.	16.6 µs	16.7 µs	
		V:Bit Reg.	16.6 µs	16.7 µs	
	K:Constant	12.0 µs	12.1 µs		
	P:Indir. (Data)	63.0 µs	63.1 µs		
P: Indir. (Data)	P:Indir. (Bit)	63.0 µs	63.1 µs		
	V:Data Reg.	63.2 µs	63.4 µs		
	V:Bit Reg.	63.2 µs	63.4 µs		
	K:Constant	57.4 µs	57.5 µs		
	P:Indir. (Data)	106.9 µs	107.0 µs		
	P:Indir. (Bit)	106.9 µs	107.0 µs		
P: Indir. (Bit)	V:Data Reg.	63.2 µs	63.4 µs		
	V:Bit Reg.	63.2 µs	63.4 µs		
	K:Constant	57.4 µs	57.5 µs		
	P:Indir. (Data)	106.9 µs	107.0 µs		
	P:Indir. (Bit)	106.9 µs	107.0 µs		



Appendix C: Instruction Execution Times

Comparative Boolean Instructions (cont'd)			DL05	
Instruction	Legal Data Types		Execute	Not Execute
OR	1st V: T, CT	2nd V Data Reg	16.1 µs	16.0 µs
		V:Bit Reg	16.1 µs	16.0 µs
	V: Data Reg.	K:Constant	11.3 µs	11.2 µs
		P:Indir. (Data)	62.4 µs	62.2 µs
		P:Indir. (Bit)	62.4 µs	62.2 µs
		V:Data Reg.	16.1 µs	16.0 µs
		V:Bit Reg	16.1 µs	16.0 µs
		K:Constant	11.3 µs	11.3 µs
	V: Bit Reg.	P:Indir. (Data)	62.4 µs	62.2 µs
		P:Indir. (Bit)	62.4 µs	62.2 µs
		V:Data Reg.	16.1 µs	16.0 µs
		V:Bit Reg	16.1 µs	16.0 µs
		K:Constant	11.3 µs	11.2 µs
		P:Indir. (Data)	62.4 µs	62.2 µs
	P: Indir. (Data)	P:Indir. (Bit)	62.4 µs	62.2 µs
		V:Data Reg	62.6 µs	62.5 µs
		V:Bit Reg	62.6 µs	62.5 µs
		K:Constant	56.8 µs	56.7 µs
		P:Indir. (Data)	106.4 µs	106.2 µs
		P:Indir. (Bit)	106.4 µs	106.2 µs
	P: Indir. (Bit)	V:Data Reg	62.6 µs	62.5 µs
		V:Bit Reg	62.6 µs	62.5 µs
		K:Constant	56.8 µs	56.7 µs
		P:Indir. (Data)	106.4 µs	106.2 µs
P:Indir. (Bit)		106.4 µs	106.2 µs	
ORN	1st V: T, CT	2nd V:Data Reg.	16.2 µs	16.3 µs
		V:Bit Reg	16.2 µs	16.3 µs
	V: Data Reg	K:Constant	11.5 µs	11.6 µs
		P:Indir. (Data)	62.5 µs	62.6 µs
		P:Indir. (Bit)	62.5 µs	62.6 µs
		V:Data Reg	16.2 µs	16.3 µs
		V:Bit Reg	16.2 µs	16.3 µs
		K:Constant	11.5 µs	11.6 µs
	V: Bit Reg.	P:Indir. (Data)	62.5 µs	62.6 µs
		P:Indir. (Bit)	62.5 µs	62.6 µs
		V:Data Reg.	16.2 µs	16.3 µs
		V:Bit Reg.	16.2 µs	16.3 µs
		K:Constant	11.5 µs	11.6 µs
		P:Indir. (Data)	62.5 µs	62.6 µs
	P: Indir. (Data)	P:Indir. (Bit)	62.5 µs	62.6 µs
		V:Data Reg.	62.7 µs	62.9 µs
		V:Bit Reg.	62.7 µs	62.9 µs
		K:Constant	57.0 µs	57.1 µs
		P:Indir. (Data)	106.5 µs	106.6 µs
		P:Indir. (Bit)	106.5 µs	106.6 µs
	P: Indir. (Bit)	V:Data Reg.	62.7 µs	62.9 µs
		V:Bit Reg.	62.7 µs	62.9 µs
		K:Constant	57.0 µs	57.1 µs
		P:Indir. (Data)	106.5 µs	106.6 µs
P:Indir. (Bit)		106.5 µs	106.6 µs	

Appendix C: Instruction Execution Times

Comparative Boolean Instructions (cont'd)			DL05	
Instruction	Legal Data Types		Execute	Not Execute
AND	1st V: T, CT	2nd V Data Reg.	16.1 µs	16.0 µs
		V:Bit Reg	16.1 µs	16.0 µs
	V: Data Reg.	K:Constant	11.3 µs	11.2 µs
		P:Indir. (Data)	62.4 µs	62.2 µs
		P:Indir. (Bit)	62.4 µs	62.2 µs
		V:Data Reg	16.1 µs	16.0 µs
		V:Bit Reg	16.1 µs	16.0 µs
		K:Constant	11.3 µs	11.2 µs
	V: Bit Reg.	P:Indir. (Data)	62.4 µs	62.2 µs
		P:Indir. (Bit)	62.4 µs	62.2 µs
		V:Data Reg.	16.1 µs	16.0 µs
		V:Bit Reg	16.1 µs	16.0 µs
		K:Constant	11.3 µs	11.2 µs
		P:Indir. (Data)	62.4 µs	62.2 µs
	P: Indir. (Data)	P:Indir. (Bit)	62.4 µs	62.2 µs
		V:Data Reg	62.6 µs	62.5 µs
		V:Bit Reg	62.6 µs	62.5 µs
		K:Constant	56.8 µs	56.7 µs
		P:Indir. (Data)	106.4 µs	106.2 µs
		P:Indir. (Bit)	106.4 µs	106.2 µs
	P: Indir. (Bit)	V:Data Reg	62.6 µs	62.5 µs
		V:Bit Reg	62.6 µs	62.5 µs
		K:Constant	56.8 µs	56.7 µs
		P:Indir. (Data)	106.4 µs	106.2 µs
P:Indir. (Bit)		106.4 µs	106.2 µs	
ANDN	1st V: T, CT	2nd V:Data Reg.	16.2 µs	16.4 µs
		V:Bit Reg.	16.2 µs	16.4 µs
	V: Data Reg.	K:Constant	11.5 µs	11.6 µs
		P:Indir. (Data)	62.5 µs	62.6 µs
		P:Indir. (Bit)	62.5 µs	62.6 µs
		V:Data Reg	16.2 µs	16.4 µs
		V:Bit Reg.	16.2 µs	16.4 µs
		K:Constant	11.5 µs	11.6 µs
	V: Bit Reg.	P:Indir. (Data)	62.5 µs	62.6 µs
		P:Indir. (Bit)	62.5 µs	62.6 µs
		V:Data Reg.	16.2 µs	16.4 µs
		V:Bit Reg.	16.2 µs	16.4 µs
		K:Constant	11.5 µs	11.6 µs
		P:Indir. (Data)	62.5 µs	62.6 µs
	P: Indir. (Data)	P:Indir. (Bit)	62.5 µs	62.6 µs
		V:Data Reg.	62.8 µs	62.9 µs
		V:Bit Reg.	62.8 µs	62.9 µs
		K:Constant	57.0 µs	57.1 µs
		P:Indir. (Data)	106.5 µs	106.6 µs
		P:Indir. (Bit)	106.5 µs	106.6 µs
	P: Indir. (Bit)	V:Data Reg.	62.8 µs	62.9 µs
		V:Bit Reg.	62.8 µs	62.9 µs
		K:Constant	57.0 µs	57.1 µs
		P:Indir. (Data)	106.5 µs	106.6 µs
P:Indir. (Bit)		106.5 µs	106.6 µs	



Appendix C: Instruction Execution Times

Immediate Instructions

Immediate Instructions		DL05	
Instruction	Legal Data Types	Execute	Not Execute
STRI	X	51.87 µs	0.0
STRNI	X	52.0 µs	0.0
ORI	X	51.87 µs	0.0
ORNI	X	51.9 µs	0.0
ANDI	X	51.87 µs	0.0
ANDNI	X	51.9 µs	0.0
OUTI	Y	96.0 µs	0.0
OROUTI	Y	105.0 µs	0.0
SETI	1st #: Y	84.0 µs	0.0
	2nd #: Y (Npt)	147.4 µs + 5 µs x N	0.0
RSTI	1st #: Y	84.0 µs	0.0
	2nd #: Y (Npt)	147.5 µs + 5 µs x N	0.0

Timer, Counter and Shift Register

Timer, Counter, and Shift Register			DL05	
Instruction	Legal Data Types		Execute	Not Execute
TMR	1st T	2nd V:Data Reg.	74.23 µs	70.5 µs
		V:Bit Reg.	74.23 µs	70.5 µs
		K:Constant	68.83 µs	64.7 µs
		P:Indir. (Data)	123.0 µs	119.3 µs
		P:Indir. (Bit)	123.0 µs	119.3 µs
TMRF	1st T	2nd V:Data Reg.	145.23 µs	70.5 µs
		V:Bit Reg.	145.23 µs	70.5 µs
		K:Constant	109.6 µs	64.5 µs
		P:Indir. (Data)	194.0 µs	119.3 µs
		P:Indir. (Bit)	194.0 µs	119.3 µs
TMRA	1st T	2nd V:Data Reg.	118.87 µs	73.4 µs
		V:Bit Reg.	118.87 µs	73.4 µs
		K:Constant	111.33 µs	66.75 µs
		P:Indir. (Data)	166.9 µs	128.1 µs
		P:Indir. (Bit)	166.9 µs	128.1 µs
TMRAF	1st T	2nd V:Data Reg.	148.53 µs	73.4 µs
		V:Bit Reg.	148.53 µs	73.4 µs
		K:Constant	142.30 µs	66.7 µs
		P:Indir. (Data)	197.3 µs	128.15 µs
		P:Indir. (Bit)	197.3 µs	128.15 µs
CNT	1st T	2nd V:Data Reg.	102.53 µs	81.5 µs
		V:Bit Reg.	102.53 µs	81.5 µs
		K:Constant	97.1 µs	76.1 µs
		P:Indir. (Data)	151.4 µs	130.4 µs
		P:Indir. (Bit)	151.4 µs	130.4 µs

Timer, Counter, and Shift Register, (cont,d)			DL05	
Instruction	Legal Data Types		Execute	Not Execute
SGCNT	CT	1st		
		2nd		
		V:Data Reg.	100.0 µs	92.4 µs
		V:Bit Reg.	100.0 µs	92.4 µs
		K:Constant	64.6 µs	87.0 µs
UDC	CT	P:Indir. (Data)	148.90 µs	141.30 µs
		P:Indir. (Bit)	148.90 µs	141.30 µs
UDC	CT	1st		
		2nd		
		V:Data Reg.	139.87 µs	120.20 µs
		V:Bit Reg.	139.87 µs	120.20 µs
		K:Constant	133.73 µs	114.15 µs
SR	C (N points to shift)	P:Indir. (Data)	188.80 µs	169.10 µs
		P:Indir. (Bit)	188.80 µs	169.10 µs
			49.0 µs + 4.9 µs x N	39.15 µs



Accumulator Data Instructions

Accumulator / Stack Load and Output Data Instructions			DL05	
Instruction	Legal Data Types		Execute	Not Execute
LD		V:Data Reg.	47.0 µs	3.9 µs
		V:Bit Reg.	47.0 µs	3.9 µs
		K:Constant	41.37 µs	3.3 µs
		P:Indir. (Data)	93.3 µs	3.2 µs
		P:Indir. (Bit)	93.3 µs	3.2 µs
LDD		V:Data Reg.	46.6 µs	3.35 µs
		V:Bit Reg.	46.6 µs	3.35 µs
		K:Constant	41.5 µs	3.35 µs
		P:Indir. (Data)	93.8 µs	3.4 µs
		P:Indir. (Bit)	93.8 µs	3.4 µs
LDF	1st X, Y, C, S,T, CT,SP	2nd K:Constant (N pt)	78.0 µs + 3.3 µs x N	4.4 µs
LDA	O: (Octal constant for address)		41.37 µs	3.3 µs
OUT		V:Data Reg.	14.4 µs	3.2 µs
		V:Bit Reg.	14.4 µs	3.2 µs
		P:Indir. (Data)	61.6 µs	3.3 µs
		P:Indir. (Bit)	61.6 µs	3.3 µs
OUTD		V:Data Reg.	17.3 µs	3.4 µs
		V:Bit Reg.	17.3 µs	3.4 µs
		P:Indir. (Data)	65.27 µs	3.35 µs
		P:Indir. (Bit)	65.27 µs	3.35 µs
OUTF	1st X, Y, C	2nd K:Constant (N pt)	49.8 µs + 5.4 µs x N	4.3 µs
POP	None		42.3 µs	2.2 µs

Appendix C: Instruction Execution Times

Logical Instructions

Logical (Accumulator) Instructions		DL05	
Instruction	Legal Data Types	Execute	Not Execute
AND	V:Data Reg.	23.63 μ s	3.4 μ s
	V:Bit Reg.	23.63 μ s	3.4 μ s
	P:Indir. (Data)	68.1 μ s	3.4 μ s
	P:Indir. (Bit)	68.1 μ s	3.4 μ s
ANDD	V:Data Reg.	23.4 μ s	3.25 μ s
	V:Bit Reg.	23.4 μ s	3.25 μ s
	K:Constant	19.27 μ s	3.35 μ s
	P:Indir. (Data)	70.0 μ s	3.4 μ s
	P:Indir. (Bit)	70.0 μ s	3.4 μ s
OR	V:Data Reg.	23.50 μ s	3.25 μ s
	V:Bit Reg.	23.50 μ s	3.25 μ s
	P:Indir. (Data)	69.77 μ s	3.2 μ s
	P:Indir. (Bit)	69.77 μ s	3.2 μ s
ORD	V:Data Reg.	23.9 μ s	3.35 μ s
	V:Bit Reg.	23.9 μ s	3.35 μ s
	K:Constant	19.13 μ s	3.3 μ s
	P:Indir. (Data)	69.8 μ s	3.25 μ s
	P:Indir. (Bit)	69.8 μ s	3.25 μ s
XOR	V:Data Reg.	23.6 μ s	3.3 μ s
	V:Bit Reg.	23.6 μ s	3.3 μ s
	P:Indir. (Data)	69.83 μ s	3.4 μ s
	P:Indir. (Bit)	69.83 μ s	3.4 μ s
XORD	V:Data Reg.	23.4 μ s	3.25 μ s
	V:Bit Reg.	23.4 μ s	3.25 μ s
	K:Constant	19.27 μ s	3.4 μ s
	P:Indir. (Data)	71.0 μ s	3.4 μ s
	P:Indir. (Bit)	71.0 μ s	3.4 μ s
CMP	V:Data Reg.	22.5 μ s	3.3 μ s
	V:Bit Reg.	22.5 μ s	3.3 μ s
	P:Indir. (Data)	68.67 μ s	3.2 μ s
	P:Indir. (Bit)	68.67 μ s	3.2 μ s
CMPD	V:Data Reg.	37.9 μ s	3.4 μ s
	V:Bit Reg.	37.7 μ s	3.4 μ s
	K:Constant	33.4 μ s	3.25 μ s
	P:Indir. (Data)	84.23 μ s	3.3 μ s
	P:Indir. (Bit)	84.23 μ s	3.3 μ s

Math Instructions

Math Instructions (Accumulator)		DL05	
Instruction	Legal Data Types	Execute	Not Execute
ADD	V:Data Reg.	168.4 μ s	3.9 μ s
	V:Bit Reg.	168.4 μ s	3.9 μ s
	P:Indir. (Data)	213.08 μ s	3.9 μ s
	P:Indir. (Bit)	213.08 μ s	3.9 μ s
ADDD	V:Data Reg.	177.3 μ s	3.8 μ s
	V:Bit Reg.	177.3 μ s	3.8 μ s
	K:Constant	151.8 μ s	3.9 μ s
	P:Indir. (Data)	222.2 μ s	3.8 μ s
	P:Indir. (Bit)	222.2 μ s	3.8 μ s
SUB	V:Data Reg.	175.3 μ s	3.9 μ s
	V:Bit Reg.	175.3 μ s	3.9 μ s
	P:Indir. (Data)	219.9 μ s	3.9 μ s
	P:Indir. (Bit)	219.9 μ s	3.9 μ s

Appendix C: Instruction Execution Times

Math Instructions (Accumulator) (cont'd)		DL05	
Instruction	Legal Data Types	Execute	Not Execute
SUBD	V:Data Reg.	187.4 μ s	3.8 μ s
	V:Bit Reg.	187.4 μ s	3.8 μ s
	K:Constant	158.5 μ s	3.8 μ s
	P:Indir. (Data)	229.1 μ s	3.9 μ s
	P:Indir. (Bit)	229.1 μ s	3.9 μ s
MUL	V:Data Reg.	483.55 μ s	3.8 μ s
	V:Bit Reg.	483.55 μ s	3.8 μ s
	K:Constant	473.30 μ s	3.9 μ s
	P:Indir. (Data)	542.30 μ s	3.8 μ s
	P:Indir. (Bit)	542.30 μ s	3.8 μ s
MULD	V:Data Reg.	1594.0 μ s	3.8 μ s
	V:Bit Reg.	1594.0 μ s	3.8 μ s
	P:Indir. (Data)	1656.0 μ s	3.8 μ s
	P:Indir. (Bit)	1656.0 μ s	3.8 μ s
DIV	V:Data Reg.	707.1 μ s	3.9 μ s
	V:Bit Reg.	707.1 μ s	3.9 μ s
	K:Constant	688.3 μ s	3.8 μ s
	P:Indir. (Data)	751.6 μ s	3.8 μ s
	P:Indir. (Bit)	751.6 μ s	3.8 μ s
DIVD	V:Data Reg.	712.1 μ s	3.8 μ s
	V:Bit Reg.	712.1 μ s	3.8 μ s
	P:Indir. (Data)	754.6 μ s	3.8 μ s
	P:Indir. (Bit)	754.6 μ s	3.8 μ s
INC	V:Data Reg.	66.4 μ s	3.8 μ s
	V:Bit Reg.	66.4 μ s	3.8 μ s
	P:Indir. (Data)	109.9 μ s	3.8 μ s
	P:Indir. (Bit)	109.9 μ s	3.8 μ s
DEC	V:Data Reg.	68.2 μ s	3.8 μ s
	V:Bit Reg.	68.2 μ s	3.8 μ s
	P:Indir. (Data)	112.7 μ s	3.8 μ s
	P:Indir. (Bit)	112.7 μ s	3.8 μ s
ADDB	V:Data Reg.	70.0 μ s	3.7 μ s
	V:Bit Reg.	70.0 μ s	3.7 μ s
	K:Constant	82.9 μ s	3.8 μ s
	P:Indir. (Data)	113.9 μ s	3.8 μ s
	P:Indir. (Bit)	113.9 μ s	3.8 μ s
SUBB	V:Data Reg.	70.25 μ s	3.8 μ s
	V:Bit Reg.	70.25 μ s	3.8 μ s
	K:Constant	68.3 μ s	3.8 μ s
	P:Indir. (Data)	114.0 μ s	3.8 μ s
	P:Indir. (Bit)	114.0 μ s	3.8 μ s
MULB	V:Data Reg.	23.9 μ s	3.8 μ s
	V:Bit Reg.	23.9 μ s	3.8 μ s
	K:Constant	20.3 μ s	3.8 μ s
	P:Indir. (Data)	67.9 μ s	3.8 μ s
	P:Indir. (Bit)	67.9 μ s	3.8 μ s
DIVB	V:Data Reg.	80.9 μ s	3.8 μ s
	V:Bit Reg.	80.9 μ s	3.8 μ s
	K:Constant	77.25 μ s	3.8 μ s
	P:Indir. (Data)	124.9 μ s	3.8 μ s
	P:Indir. (Bit)	124.9 μ s	3.8 μ s

C

Appendix C: Instruction Execution Times

Math Instructions (Accumulator) (cont'd)		DL05	
Instruction	Legal Data Types	Execute	Not Execute
INCB	V:Data Reg.	23.4 μ s	3.9 μ s
	V:Bit Reg.	23.4 μ s	3.9 μ s
	P:Indir. (Data)	66.5 μ s	3.8 μ s
	P:Indir. (Bit)	66.5 μ s	3.8 μ s
DECB	V:Data Reg.	23.2 μ s	3.8 μ s
	V:Bit Reg.	23.2 μ s	3.8 μ s
	P:Indir. (Data)	67.2 μ s	3.9 μ s
	P:Indir. (Bit)	67.2 μ s	3.9 μ s

Bit Instructions

Bit Instructions (Accumulator)		DL05	
Instruction	Legal Data Types	Execute	Not Execute
SUM	None	26.9 μ s	2.6 μ s
SHFL	V:Data Reg. (N bits)	21.8 μ s	2.1 μ s
	V:Bit Reg. (N bits)	21.8 μ s	2.1 μ s
	K:Constant (N bits)	19.5 μ s	2.1 μ s
SHFR	V:Data Reg. (N bits)	21.5 μ s	2.1 μ s
	V:Bit Reg. (N bits)	21.5 μ s	2.1 μ s
	K:Constant (N bits)	19.6 μ s	2.1 μ s
ENCO	None	382.0 μ s	2.7 μ s
DECO	None	16.4 μ s	2.7 μ s

Number Conversion Instructions

Number Conversion Instructions (Accumulator)		DL05	
Instruction	Legal Data Types	Execute	Not Execute
BIN	None	159.9 μ s	2.6 μ s
BCD	None	175.0 μ s	2.6 μ s
INV	None	6.7 μ s	2.6 μ s
ATH	None	319.0 μ s	3.7 μ s
HTA	None	301.6 μ s	3.9 μ s
GRAY	None	213.4 μ s	2.7 μ s
SFLDGT	None	259.1 μ s	2.7 μ s

Table Instructions

Table Instructions		DL05	
Instruction	Legal Data Types	Execute	Not Execute
MOV	V: Data/Bit Reg. to Vdata/Bit Reg (N pt)	136.1 μ s + 20.8 μ s x N	3.25 μ s
MOVMC	V: Data/Bit Reg <=> E ² (N pt)	86.0 μ s + 30.7 μ s x N	0
LDLBLE	K: Constant	33.2 μ s	0

CPU Control Instructions

CPU Control Instructions		DL05	
Instruction	Legal Data Types	Execute	Not Execute
NOP	None	1.0 μ s	1.0 μ s
END	None	21.8 μ s	0.0
STOP	None	2.6 μ s	1.15 μ s
RSTWDT	None	6.3 μ s	2.6 μ s
NOT	None	1.6 μ s	1.6 μ s



Program Control Instructions

Program Control Instructions		DL05	
Instruction	Legal Data Types	Execute	Not Execute
FOR	V, K	202.9 μ s	15.0 μ s
NEXT	None	62.27 μ s	-
GTS	K: Constant	27.6 μ s	15.3 μ s
SBR	K: Constant	1.6 μ s	0.0
RTC	None	25.7 μ s	12.1 μ s
RT	None	21.6 μ s	0.0
MLS	K: Constant	35.6 μ s	35.6 μ s
MLR	K: Constant	15.4 μ s	15.4 μ s

Interrupt Instructions

Interrupt Instructions		DL05	
Instruction	Legal Data Types	Execute	Not Execute
ENI	None	23.8 μ s	2.2 μ s
DISI	None	9.4 μ s	2.3 μ s
INT	0	7.5 μ s	0
IRT	None	6.6 μ s	0
IRTC	None	0.9 μ s	1.3 μ s

Network Instructions

Network Instructions		DL05	
Instruction	Legal Data Types	Execute	Not Execute
RX	X, Y, C, T, CT, SP, S, V	1639.0 μ s	4.2 μ s
	V:Data Reg.	1639.0 μ s	4.2 μ s
	V:Bit Reg.	1639.0 μ s	4.2 μ s
	P:Indir. (Data)	1674.0 μ s	4.2 μ s
	P:Indir. (Bit)	1674.0 μ s	4.2 μ s
WX	X, Y, C, T, CT, SP, S, V	1691.0 μ s	4.2 μ s
	V:Data Reg.	1691.0 μ s	4.2 μ s
	V:Bit Reg.	1691.0 μ s	4.2 μ s
	P:Indir. (Data)	1726.0 μ s	4.2 μ s
	P:Indir. (Bit)	1726.0 μ s	4.2 μ s

Appendix C: Instruction Execution Times

Message Instructions

Message Instructions		DL05	
Instruction	Legal Data Types	Execute	Not Execute
FAULT	V:Data Reg.	163.5 μ s	4.2 μ s
	V:Bit Reg.	163.5 μ s	4.2 μ s
	K:Constant	204.4 μ s	4.3 μ s
DLBL	K: Constant	–	0.0
NCON	K: Constant	–	0.0
ACON	K: Constant	–	0.0
PRINT		817.23 μ s	3.8 μ s

RLL^{PLUS} Instructions

RLL ^{PLUS} Instructions		DL05	
Instruction	Legal Data Types	Execute	Not Execute
ISG	S	57.27 μ s	54.4 μ s
SG	S	57.25 μ s	54.4 μ s
JMP	S	109.2 μ s	8.9 μ s
NJMP	S	109.2 μ s	8.9 μ s
CV	S	38.9 μ s	38.9 μ s
CVJMP	S	26.0 μ s	26.0 μ s

Drum Instructions

Drum Instructions		DL05	
Instruction	Legal Data Types	Execute	Not Execute
DRUM	CT	1204.0 μ s	398.2 μ s
EDRUM	CT	989.2 μ s	421.05 μ s

Word Bit Instructions

Word Bit Instructions		DL05	
Instruction	Legal Data Types	Execute	Not Execute
STRB	V:Data Reg.	5.6 μ s	5.6 μ s
	V:Bit Reg.	5.6 μ s	5.6 μ s
	P:Indir. (Data)	30.8 μ s	30.8 μ s
	P:Indir. (Bit)	64.4 μ s	64.4 μ s
STRNB	V:Data Reg.	5.6 μ s	5.6 μ s
	V:Bit Reg.	5.5 μ s	5.5 μ s
	P:Indir. (Data)	30.7 μ s	30.7 μ s
	P:Indir. (Bit)	64.4 μ s	64.4 μ s
ORB	V:Data Reg.	5.5 μ s	5.5 μ s
	V:Bit Reg.	5.5 μ s	5.5 μ s
	P:Indir. (Data)	30.9 μ s	30.9 μ s
	P:Indir. (Bit)	64.5 μ s	64.5 μ s
ORNB	V:Data Reg.	5.6 μ s	5.6 μ s
	V:Bit Reg.	5.5 μ s	5.5 μ s
	P:Indir. (Data)	30.9 μ s	30.9 μ s
	P:Indir. (Bit)	64.5 μ s	64.5 μ s
ANDB	V:Data Reg.	5.6 μ s	5.6 μ s
	V:Bit Reg.	5.5 μ s	5.5 μ s
	P:Indir. (Data)	30.9 μ s	30.9 μ s
	P:Indir. (Bit)	64.5 μ s	64.5 μ s
ANDNB	V:Data Reg.	5.6 μ s	5.6 μ s
	V:Bit Reg.	5.6 μ s	5.6 μ s
	P:Indir. (Data)	30.9 μ s	30.9 μ s
	P:Indir. (Bit)	64.6 μ s	64.5 μ s
OUTB	V:Data Reg.	11.4 μ s	11.5 μ s
	V:Bit Reg.	11.4 μ s	11.5 μ s
	P:Indir. (Data)	36.7 μ s	36.7 μ s
	P:Indir. (Bit)	70.2 μ s	70.4 μ s
SETB	V:Data Reg.	9.5 μ s	4.7 μ s
	V:Bit Reg.	9.5 μ s	4.8 μ s
	P:Indir. (Data)	34.7 μ s	30.0 μ s
	P:Indir. (Bit)	68.4 μ s	63.7 μ s
RSTB	V:Data Reg.	9.8 μ s	4.8 μ s
	V:Bit Reg.	9.8 μ s	4.7 μ s
	P:Indir. (Data)	35.1 μ s	30.0 μ s
	P:Indir. (Bit)	68.7 μ s	63.7 μ s

