

# Instruction Execution Times

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## Introduction

This appendix contains several tables that provide the instruction execution times for the DL350 CPU. You will notice is that many of the execution times depend on the type of data being used with the instruction. For example, a few of the instructions that use V-memory locations are further defined by the following items.

- Data Registers
- Bit Registers

### V-Memory Data Registers

Some V-memory locations are considered data registers. For example, the V-memory locations that store the timer or counter current values, or just regular user V memory would be considered as a V-memory data register. Don't think that you cannot load a bit pattern into these types of registers, you can. It's just that their primary use is as a data register. The following locations are considered as data registers.

Data Registers	DL350
Timer Current Values	V0 – V377
Counter Current Values	V1000 – V1177
User Data Words	V1400 – V7377 V10000 – V17777

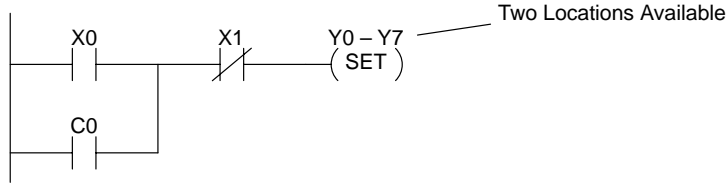
### V-Memory Bit Registers

You may recall that some of the discrete points such as X, Y, C, etc. are automatically mapped into V memory. The following locations that contain this data are considered bit registers.

Bit Registers	DL350
Input Points (X)	V40400 – V 40437
Output Points (Y)	V40500 – V40537
Control Relays (C)	V40600 – V40677
Timer Status Bits	V41100 – V41117
Counter Status Bits	V41040 – V41147
Stages	V41000 – V41077

**How to Read the Tables**

Some of the instructions can have more than one parameter so the table shows execution times that depend on the amount and type of parameters. For example, the SET instruction can be used to set a single point or a range of points. If you examine the execution table you'll notice the available data types and execution times for both situations. The following diagram shows an example.



SET	1st #:	X, Y, C, S	17.4 $\mu$ s
	2nd #:	X, Y, C, S, (N pt)	12.0 $\mu$ s+5.4 $\mu$ sxN
RST	1st #:	X, Y, C, S	19.5 $\mu$ s
	2nd #:	X, Y, C, S, (N pt)	10.5 $\mu$ s+5.2 $\mu$ sxN

Execution depends on numbers of locations and types of data used

## Boolean Instructions

Boolean Instructions		DL350	
Instruction	Legal Data Types	Execute	Not Exec
STR	X, Y, C, T, CT, S, SP	.74 $\mu$ s	.74 $\mu$ s
STRN	X, Y, C, T, CT, S, SP	0.68 $\mu$ s	0.74 $\mu$ s
OR	X, Y, C, T, CT, S, SP	0.56 $\mu$ s	0.56 $\mu$ s
ORN	X, Y, C, T, CT, S, SP	0.6 $\mu$ s	0.6 $\mu$ s
AND	X, Y, C, T, CT, S, SP	0.46 $\mu$ s	0.46 $\mu$ s
ANDN	X, Y, C, T, CT, S, SP	0.56 $\mu$ s	0.56 $\mu$ s
ANDSTR	None	0.4 $\mu$ s	0.4 $\mu$ s
ORSTR	None	0.4 $\mu$ s	0.4 $\mu$ s
OUT	X, Y, C	2.0 $\mu$ s	2.0 $\mu$ s
OUTH	X, Y, C	1.1 $\mu$ s	1.1 $\mu$ s
OROUT	X, Y, C	2.4 $\mu$ s	2.4 $\mu$ s
PD	X, Y, C	16.6 $\mu$ s	16.6 $\mu$ s
SET	1st #: X, Y, C, S	10.6 $\mu$ s	1.1 $\mu$ s
	2nd #: X, Y, C, S (N pt)	11.4 $\mu$ s+ 0.9 $\mu$ sxN	1.1 $\mu$ s
RST	1st #: X, Y, C, S	10.6 $\mu$ s	1.1 $\mu$ s
	2nd #: X, Y, C, S (N pt)	11.4 $\mu$ s+ 0.9 $\mu$ sxN	1.1 $\mu$ s
	1st #: T, CT	10.6 $\mu$ s	1.1 $\mu$ s
	2nd #: T, CT (N pt)	11.4 $\mu$ s+ 0.9 $\mu$ sxN	1.1 $\mu$ s

## Comparative Boolean

Comparative Boolean Instructions			DL350	
Instruction	Legal Data Types		Execute	Not Exec
STRE	1st V: Data Reg.	2nd V:Data Reg.	8.7μs	8.7μs
		V:Bit Reg.	5.5μs	5.5μs
		K:Constant P:Indir. (Data) P:Indir. (Bit)	35.9μs	35.9μs
	V: Bit Reg.	V:Data Reg.	8.7μs	8.7μs
		V:Bit Reg.	5.5μs	5.5μs
		K:Constant P:Indir. (Data) P:Indir. (Bit)	35.9μs	35.9μs
	P:Indir. (Data)	V:Data Reg.	—	35.6μs
		V:Bit Reg.	35.6μs	35.6μs
		K:Constant P:Indir. (Data) P:Indir. (Bit)	32.6μs 60.7μs	32.6μs 60.7μs
	P:Indir. (Bit)	V:Data Reg.	35.6μs	35.6μs
		V:Bit Reg.	35.6μs	—
		K:Constant P:Indir. (Data) P:Indir. (Bit)	32.6μs 60.7μs	32.6μs 60.7μs
STRNE	1st V: Data Reg.	2nd V:Data Reg.	8.7μs	8.7μs
		V:Bit Reg.	5.5μs	5.5μs
		K:Constant P:Indir. (Data) P:Indir. (Bit)	35.9μs	35.9μs
	V: Bit Reg.	V:Data Reg.	8.7μs	8.7μs
		V:Bit Reg.	5.5μs	5.5μs
		K:Constant P:Indir. (Data) P:Indir. (Bit)	35.9μs	35.9μs
	P:Indir. (Data)	V:Data Reg.	—	—
		V:Bit Reg.	35.6μs	35.6μs
		K:Constant P:Indir. (Data) P:Indir. (Bit)	32.6μs 60.7μs	32.6μs 60.7μs
	P:Indir. (Bit)	V:Data Reg.	35.6μs	35.6μs
		V:Bit Reg.	35.6μs	—
		K:Constant P:Indir. (Data) P:Indir. (Bit)	32.6μs 60.7μs	32.6μs 60.7μs

Comparative Boolean (cont.)			DL350	
Instruct	Legal Data Types		Execute	Not Exec
ORE	1st V: Data Reg.	2nd V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant	35.9µs	35.9µs
	V: Bit Reg.	2nd V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant	35.9µs	35.9µs
	P:Indir. (Data)	2nd V:Data Reg.	—	—
		V:Bit Reg.	35.6µs	35.6µs
		K:Constant	32.6µs	32.6µs
	P:Indir. (Bit)	2nd V:Data Reg.	60.7µs	60.7µs
		V:Bit Reg.	35.6µs	35.6µs
		K:Constant	32.6µs	32.6µs
ORNE	1st V: Data Reg.	2nd V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant	35.9µs	35.9µs
	V: Bit Reg.	2nd V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant	35.9µs	35.9µs
	P:Indir. (Data)	2nd V:Data Reg.	—	—
		V:Bit Reg.	35.6µs	35.6µs
		K:Constant	32.6µs	32.6µs
	P:Indir. (Bit)	2nd V:Data Reg.	60.7µs	60.7µs
		V:Bit Reg.	35.6µs	35.6µs
		K:Constant	32.6µs	32.6µs

Comparative Boolean (cont.)			DL350	
Instruct	Legal Data Types		Execute	Not Exec
ANDE	1st V: Data Reg.	2nd V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant P:Indir. (Data) P:Indir. (Bit)	35.9µs	35.9µs
	V: Bit Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant P:Indir. (Data) P:Indir. (Bit)	35.9µs	35.9µs
	P:Indir. (Data)	V:Data Reg.	—	—
		V:Bit Reg.	35.6µs	35.6µs
		K:Constant P:Indir. (Data) P:Indir. (Bit)	32.6µs 60.7µs	32.6µs 60.7µs
	P:Indir. (Bit)	V:Data Reg.	35.6µs	35.6µs
		V:Bit Reg.	32.6µs	32.6µs
		K:Constant P:Indir. (Data) P:Indir. (Bit)	60.7µs	60.7µs
ANDNE	1st V: Data Reg.	2nd V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant P:Indir. (Data) P:Indir. (Bit)	35.9µs	35.9µs
	V: Bit Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant P:Indir. (Data) P:Indir. (Bit)	35.9µs	35.9µs
	P:Indir. (Data)	V:Data Reg.	—	—
		V:Bit Reg.	35.6µs	35.6µs
		K:Constant P:Indir. (Data) P:Indir. (Bit)	32.6µs 60.7µs 35.6µs	32.6µs 60.7µs 35.6µs
	P:Indir. (Bit)	V:Data Reg.	32.6µs	32.6µs
		V:Bit Reg.	60.7µs	60.7µs
		K:Constant P:Indir. (Data) P:Indir. (Bit)	35.6µs	35.6µs

Comparative Boolean (cont.)			DL350		
Instruc	Legal Data Types		Execute	Not Exec	
STR	1st T, CT	2nd V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs  5.5µs 35.9µs	8.7µs  5.5µs 35.9µs	
	1st V: Data Reg.	2nd V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs  5.5µs 35.9µs	8.7µs  5.5µs 35.9µs	
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs  5.5µs 35.9µs	8.7µs  5.5µs 35.9µs	
	P:Indir. (Data)	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	— 35.6µs 32.6µs 60.7µs	— 35.6µs 32.6µs 60.7µs	
	P:Indir. (Bit)	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	35.6µs  32.6µs 60.7µs	35.6µs  32.6µs 60.7µs	
	STRN	1st T, CT	2nd V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs  5.5µs 35.9µs	8.7µs  5.5µs 35.9µs
		1st V: Data Reg.	2nd V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs  5.5µs 35.9µs	8.7µs  5.5µs 35.9µs
		V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs  5.5µs 35.9µs	8.7µs  5.5µs 35.9µs
	P:Indir. (Data)	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	— 35.6µs 32.6µs 60.7µs	— 35.6µs 32.6µs 60.7µs	
	P:Indir. (Bit)	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	35.6µs  32.6µs 60.7µs	35.6µs  32.6µs 60.7µs	

Comparative Boolean (cont.)			DL350	
Instruc	Legal Data Types		Execute	Not Exec
OR	1st T, CT	2nd V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant	35.9µs	35.9µs
		P:Indir. (Data)		
		P:Indir. (Bit)		
	1st V: Data Reg.	2nd V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant	35.9µs	35.9µs
	P:Indir. (Data)			
	P:Indir. (Bit)			
V: Bit Reg.	2nd V:Data Reg.	8.7µs	8.7µs	
	V:Bit Reg.	5.5µs	5.5µs	
	K:Constant	35.9µs	35.9µs	
	P:Indir. (Data)			
	P:Indir. (Bit)			
P:Indir. (Data)	2nd V:Data Reg.	—	—	
	V:Bit Reg.	35.6µs	35.6µs	
	K:Constant	32.6µs	32.6µs	
	P:Indir. (Data)	60.7µs	60.7µs	
	P:Indir. (Bit)			
P:Indir. (Bit)	2nd V:Data Reg.	35.6µs	35.6µs	
	V:Bit Reg.	32.6µs	32.6µs	
	K:Constant	60.7µs	60.7µs	
	P:Indir. (Data)			
	P:Indir. (Bit)			
ORN	1st T, CT	2nd V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant	35.9µs	35.9µs
		P:Indir. (Data)		
		P:Indir. (Bit)		
	1st V: Data Reg.	2nd V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant	35.9µs	35.9µs
	P:Indir. (Data)			
	P:Indir. (Bit)			
V: Bit Reg.	2nd V:Data Reg.	8.7µs	8.7µs	
	V:Bit Reg.	5.5µs	5.5µs	
	K:Constant	35.9µs	35.9µs	
	P:Indir. (Data)			
	P:Indir. (Bit)			
P:Indir. (Data)	2nd V:Data Reg.	—	—	
	V:Bit Reg.	35.6µs	35.6µs	
	K:Constant	32.6µs	32.6µs	
	P:Indir. (Data)	60.7µs	60.7µs	
	P:Indir. (Bit)			
P:Indir. (Bit)	2nd V:Data Reg.	35.6µs	35.6µs	
	V:Bit Reg.	32.6µs	32.6µs	
	K:Constant	60.7µs	60.7µs	
	P:Indir. (Data)			
	P:Indir. (Bit)			

Comparative Boolean (cont.)			DL350	
Instruc	Legal Data Types		Execute	Not Exec
AND	1st T, CT	2nd V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant	35.9µs	35.9µs
		P:Indir. (Data)		
		P:Indir. (Bit)		
	1st V: Data Reg.	2nd V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant	35.9µs	35.9µs
		P:Indir. (Data)		
		P:Indir. (Bit)		
V: Bit Reg.	2nd V:Data Reg.	8.7µs	8.7µs	
	V:Bit Reg.	5.5µs	5.5µs	
	K:Constant	35.9µs	35.9µs	
	P:Indir. (Data)			
	P:Indir. (Bit)			
P:Indir. (Data)	2nd V:Data Reg.	—	—	
	V:Bit Reg.	35.6µs	35.6µs	
	K:Constant	32.6µs	32.6µs	
	P:Indir. (Data)	60.7µs	60.7µs	
	P:Indir. (Bit)			
P:Indir. (Bit)	2nd V:Data Reg.	35.6µs	35.6µs	
	V:Bit Reg.	32.6µs	32.6µs	
	K:Constant	60.7µs	60.7µs	
	P:Indir. (Data)			
	P:Indir. (Bit)			
ANDN	1st T, CT	2nd V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant	35.9µs	35.9µs
		P:Indir. (Data)		
		P:Indir. (Bit)		
	1st V: Data Reg.	2nd V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.	5.5µs	5.5µs
		K:Constant	35.9µs	35.9µs
		P:Indir. (Data)		
		P:Indir. (Bit)		
V: Bit Reg.	2nd V:Data Reg.	8.7µs	8.7µs	
	V:Bit Reg.	5.5µs	5.5µs	
	K:Constant	35.9µs	35.9µs	
	P:Indir. (Data)			
	P:Indir. (Bit)			
P:Indir. (Data)	2nd V:Data Reg.	—	—	
	V:Bit Reg.	35.6µs	35.6µs	
	K:Constant	32.6µs	32.6µs	
	P:Indir. (Data)	60.7µs	60.7µs	
	P:Indir. (Bit)			
P:Indir. (Bit)	2nd V:Data Reg.	35.6µs	35.6µs	
	V:Bit Reg.	32.6µs	32.6µs	
	K:Constant	60.7µs	60.7µs	
	P:Indir. (Data)			
	P:Indir. (Bit)			

## Immediate Instructions

Immediate Instructions		DL350	
Instruc	Legal Data Types	Execute	Not Exec
STRI	X	78.6 $\mu$ s	78.6 $\mu$ s
STRNI	X	78.6 $\mu$ s	78.6 $\mu$ s
ORI	X	78.6 $\mu$ s	78.6 $\mu$ s
ORNI	X	78.6 $\mu$ s	78.6 $\mu$ s
ANDI	X	78.6 $\mu$ s	78.6 $\mu$ s
ANDNI	X	78.6 $\mu$ s	78.6 $\mu$ s
OUTI	Y	91.0 $\mu$ s	91.0 $\mu$ s
OROUTI	Y	94.0 $\mu$ s	94.0 $\mu$ s
SETI	1st #: Y	87.6 $\mu$ s	1.1 $\mu$ s
	2nd #: Y (N pt)	97.5 $\mu$ s+ 16.25xN	1.1 $\mu$ s
RSTI	1st #: Y	87.6 $\mu$ s	1.1 $\mu$ s
	2nd #: Y (N pt)	97.5 $\mu$ s+ 16.25xN	

## Timer, Counter, Shift Register Instructions

Timer, Counter, Shift Register Instructions			DL350	
Instruc	Legal Data Types		Execute	Not Exec
TMR	1st	2nd		
	T	V:Data Reg.	38.6µs	24.6µs
		V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	23.0µs 54.3µs	24.6µs 52.0µs
TMRF	1st	2nd		
	T	V:Data Reg.	61.2µs	23.0µs
		V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	57.6µs 90.4µs	19.4µs 37.5µs
TMRA	1st	2nd		
	T	V:Data Reg.	58.2µs	27.1µs
		V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	53.6µs 90.4µs	22.4µs 59.2µs
TMRAF	1st	2nd		
	T	V:Data Reg.	64.5µs	27.6µs
		V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	59.9µs 96.7µs	22.4µs 59.2µs
CNT	1st	2nd		
	CT	V:Data Reg.	36.1µs	24.6µs
		V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	32.5µs 97.1µs	21.0µs 56.8µs
SGCNT	1st	2nd		
	CT	V:Data Reg.	35.2µs	27.7µs
		V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	33.7µs 67.4µs	27.1µs 57.9µs
UDC	1st	2nd		
	CT	V:Data Reg.	47.4µs	40.0µs
		V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	42.7µs 81.7µs	35.3µs 72.1µs
SR	C (N points to shift)		17.8µs+	12.6 µs
			1.0µs×N	

## Accumulator Data Instructions

Accumulator / Stack Load and Output Data Instructions		DL350	
Instruc	Legal Data Types	Execute	Not Exec
LD	V:Data Reg.	13.6 $\mu$ s	1.1 $\mu$ s
	V:Bit Reg.		
	K:Constant	10.4 $\mu$ s	1.1 $\mu$ s
	P:Indir. (Data) P:Indir. (Bit)	40.4 $\mu$ s	1.1 $\mu$ s
LDD	V:Data Reg.	14.0 $\mu$ s	1.1 $\mu$ s
	V:Bit Reg.		
	K:Constant	10.4 $\mu$ s	1.1 $\mu$ s
	P:Indir. (Data) P:Indir. (Bit)	45.0 $\mu$ s	1.3 $\mu$ s
LDF	1st	10.5 $\mu$ s+ 3.45 $\mu$ s x N	1.4 $\mu$ s
	2nd X, Y, C, S T, CT, SP K:Constant		
LDA	O: (Octal constant for address)	10.4 $\mu$ s	1.1 $\mu$ s
LDSX	K: Constant	14.6 $\mu$ s	1.5 $\mu$ s
OUT	V:Data Reg.	10.7 $\mu$ s	1.1 $\mu$ s
	V:Bit Reg.		
	P:Indir. (Data) P:Indir. (Bit)	41.9 $\mu$ s	
OUTD	V:Data Reg.	11.7 $\mu$ s	1.1 $\mu$ s
	V:Bit Reg.		
	P:Indir. (Data) P:Indir. (Bit)	42.6 $\mu$ s	
OUTF	1st	43.8 $\mu$ s+ 6.2 $\mu$ s x N	1.1 $\mu$ s
	2nd X, Y, C K:Constant		
POP	None	7.8 $\mu$ s	1.0 $\mu$ s

## Logical Instructions

Logical (Accumulator) Instructions		DL350	
Instruc	Legal Data Types	Execute	Not Exec
AND	V:Data Reg.	9.1 $\mu$ s	1.1 $\mu$ s
	V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	39.8 $\mu$ s	1.1 $\mu$ s
ANDD	V:Data Reg.	10.2 $\mu$ s	1.1 $\mu$ s
	V:Bit Reg.	6.5 $\mu$ s	1.1 $\mu$ s
	K:Constant	40.9 $\mu$ s	1.1 $\mu$ s
	P:Indir. (Data) P:Indir. (Bit)		
OR	V:Data Reg.	9.3 $\mu$ s	1.1 $\mu$ s
	V:Bit Reg.	40.2 $\mu$ s	1.1 $\mu$ s
	P:Indir. (Data)		
	P:Indir. (Bit)		
ORD	V:Data Reg.	10.4 $\mu$ s	1.1 $\mu$ s
	V:Bit Reg.	6.7 $\mu$ s	1.1 $\mu$ s
	K:Constant	41.1 $\mu$ s	1.1 $\mu$ s
	P:Indir. (Data) P:Indir. (Bit)		
XOR	V:Data Reg.	9.2 $\mu$ s	1.1 $\mu$ s
	V:Bit Reg.	40.0 $\mu$ s	1.1 $\mu$ s
	P:Indir. (Data)		
	P:Indir. (Bit)		
XORD	V:Data Reg.	10.3 $\mu$ s	1.1 $\mu$ s
	V:Bit Reg.	6.2 $\mu$ s	1.1 $\mu$ s
	K:Constant	41.0 $\mu$ s	1.1 $\mu$ s
	P:Indir. (Data) P:Indir. (Bit)		
CMP	V:Data Reg.	10.8 $\mu$ s	1.1 $\mu$ s
	V:Bit Reg.	41.5 $\mu$ s	1.1 $\mu$ s
	P:Indir. (Data)		
	P:Indir. (Bit)		
CMPD	V:Data Reg.	11.4 $\mu$ s	1.2 $\mu$ s
	V:Bit Reg.	7.7 $\mu$ s	1.2 $\mu$ s
	K:Constant	42.1 $\mu$ s	1.2 $\mu$ s
	P:Indir. (Data) P:Indir. (Bit)		
CMPS	None	—	—

## Math Instructions

Math Instructions (Accumulator)		DL350	
Instruc	Legal Data Types	Execute	Not Exec
ADD	V:Data Reg.	93.3μs	1.2μs
	V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	129.8μs	1.1μs
ADDD	V:Data Reg.	99.2μs	1.2μs
	V:Bit Reg. K:Constant	80.6μs	1.2μs
	P:Indir. (Data) P:Indir. (Bit)	129.8μs	1.2μs
SUB	V:Data Reg.	92.1μs	1.1μs
	V:Bit Reg. P:Indir. (Data)	121.9μs	1.1μs
	P:Indir. (Bit)		
SUBD	V:Data Reg.	98.2μs	1.1μs
	V:Bit Reg. K:Constant	78.6μs	1.1μs
	P:Indir. (Data)	127.8μs	1.1μs
	P:Indir. (Bit)		
MUL	V:Data Reg.	341.1μs	1.1μs
	V:Bit Reg. K:Constant	367.8	1.1μs
	P:Indir. (Data)	371.8μs	1.1μs
	P:Indir. (Bit)		
MULD	V:Data Reg.	1075.8μs	1.1μs
	V:Bit Reg. P:Indir. (Data)	1106.5μs	1.1μs
	P:Indir. (Bit)		
DIV	V:Data Reg.	466.6μs	1.1μs
	V:Bit Reg. K:Constant	492.8μs	1.1μs
	P:Indir. (Data)	538.2μs	1.1μs
	P:Indir. (Bit)		
DIVD	V:Data Reg.	510.6μs	1.1μs
	V:Bit Reg. P:Indir. (Data)	501.1μs	1.1μs
	P:Indir. (Bit)		
INCB	V:Data Reg.	15.2μs	1.1μs
	V:Bit Reg. P:Indir. (Data)	45.9μs	1.1μs
	P:Indir. (Bit)		
DECB	V:Data Reg.	15.2μs	1.1μs
	V:Bit Reg. P:Indir. (Data)	45.2μs	1.1μs
	P:Indir. (Bit)		

## Bit Instructions

Bit Instructions (Accumulator)		DL350	
Instruc	Legal Data Types	Execute	Not Exec
SHFR	V:Data Reg. (N bits)	9.8 $\mu$ s+ 0.2 x N	1.2 $\mu$ s
	V:Bit Reg. (N bits) K:Constant (N bits)	7.9 $\mu$ s+0.2 x N	
SHFL	V:Data Reg. (N bits)	9.8 $\mu$ s+ 0.2 x N	1.2 $\mu$ s
	V:Bit Reg. (N bits) K:Constant (N bits)	7.9 $\mu$ s+ 0.2 x N	
ROTR	V:Data Reg. (N bits)	15.7	1.2 $\mu$ s
	V:Bit Reg. (N bits) K:Constant (N bits)	12.3	
ROTL	V:Data Reg. (N bits)	15.7 $\mu$ s	1.2 $\mu$ s
	V:Bit Reg. (N bits) K:Constant (N bits)	12.3 $\mu$ s	
ENCO	None	40.3 $\mu$ s	1.0 $\mu$ s
DECO	None	6.5 $\mu$ s	1.0 $\mu$ s

## Number Conversion Instructions

Number Conversion Instructions (Accumulator)		DL350	
Instruc	Legal Data Types	Execute	Not Exec
BIN	None	128.4 $\mu$ s	1.0 $\mu$ s
BCD	None	122.0 $\mu$ s	1.0 $\mu$ s
INV	None	2.9 $\mu$ s	1.0 $\mu$ s
BCDCPL	None	74.5 $\mu$ s	1.0 $\mu$ s
ATH	None	29.2 $\mu$ s	1.0 $\mu$ s
HTA	None	29.2 $\mu$ s	1.0 $\mu$ s
SEG	None	12.6 $\mu$ s	1.0 $\mu$ s
GRAY	None	142.0 $\mu$ s	1.0 $\mu$ s
SFLDGT	None	26.6 $\mu$ s	1.0 $\mu$ s

## Table Instructions

Table Instructions		DL350	
Instruc	Legal Data Types	Execute	Not Exec
MOV	Move V:data reg. to V:data reg. Move V:bit reg. to V:data reg. Move V:data reg to V:bit reg. Move V:bit reg. to V:bit reg. N= #of words	63 $\mu$ s+ 16xN	1.20 $\mu$ s
MOVMC	Move V:Data Reg. to E <sup>2</sup> Move V:Bit Reg. to E <sup>2</sup> Move from E <sup>2</sup> to V:Data Reg. Move from E <sup>2</sup> to V:Bit Reg. N= #of words	50 $\mu$ s+ 15xN	1.2 $\mu$ s
LDLBL	K	7.4 $\mu$ s	1.5 $\mu$ s

## CPU Control Instructions

CPU Control Instructions		DL350	
Instruc	Legal Data Types	Execute	Not Exec
NOP	None	0.6 $\mu$ s	0.6 $\mu$ s
END	None	14.7 $\mu$ s	14.7 $\mu$ s
STOP	None	4.1 $\mu$ s	1.0 $\mu$ s
RSTWT	None	5.4 $\mu$ s	1.0 $\mu$ s
NOT	None	1.0 $\mu$ s	1.0 $\mu$ s

## Program Control Instructions

Program Control Instructions		DL350	
Instruc	Legal Data Types	Execute	Not Exec
GOTO	K	5.0 $\mu$ s	4.9 $\mu$ s
LBL	K	0.6 $\mu$ s	0.6 $\mu$ s
FOR	V, K	110 $\mu$ s	7.9 $\mu$ s
NEXT	None	48.4 $\mu$ s	0 $\mu$ s
GTS	K	12.5 $\mu$ s	6.3 $\mu$ s
SBR	K	0.5 $\mu$ s	0 $\mu$ s
RT	None	11.4 $\mu$ s	11.4 $\mu$ s
MLS	K (1-7)	4.2 $\mu$ s	4.2 $\mu$ s
MLR	K (0-7)	4.0 $\mu$ s	4.0 $\mu$ s

## Interrupt Instructions

Interrupt Instructions		DL350	
Instruc	Legal Data Types	Execute	Not Exec
ENI	None	45.8 $\mu$ s	1.1 $\mu$ s
DISI	None	5.7 $\mu$ s	1.1 $\mu$ s
INT	0 (0–7)	0 $\mu$ s	0 $\mu$ s
IRT	None	1.5 $\mu$ s	—
IRTC	None	0.5 $\mu$ s	0.5

## Network Instructions

Network Instructions		DL350	
Instruc	Legal Data Types	Execute	Not Exec
RX	X, Y, C, T, CT, SP, S V:Data Reg. V:Bit Reg.	2024.1 $\mu$ s	1.4 $\mu$ s
WX	X, Y, C, T, CT, SP, S V:Data Reg. V:Bit Reg.	2024.1 $\mu$ s	1.4 $\mu$ s

## Message Instructions

Message Instructions		DL350	
Instruc	Legal Data Types	Execute	Not Exec
FAULT	V:Data Reg. V:Bit Reg. K:Constant	108.9 $\mu$ s	1.4 $\mu$ s
		108.9 $\mu$ s	1.4 $\mu$ s
		96.2 $\mu$ s	1.4 $\mu$ s
DLBL	K	0 $\mu$ s	0 $\mu$ s
NCON	K	0 $\mu$ s	$\mu$ s
ACON	K	0 $\mu$ s	0 $\mu$ s
PRINT		104.0 $\mu$ s	1.4 $\mu$ s

## RLL<sup>PLUS</sup> Instructions

RLL <sup>PLUS</sup> Instructions		DL350	
Instruc	Legal Data Types	Execute	Not Exec
ISG	S	24.3 $\mu$ s	21.5 $\mu$ s
SG	S	24.3 $\mu$ s	21.5 $\mu$ s
JMP	S	24.4 $\mu$ s	4.3 $\mu$ s
NJMP	S	24.4 $\mu$ s	4.6 $\mu$ s
CV	S	13.9 $\mu$ s	13.9 $\mu$ s
CVJMP	S (N stages, 1 to 16)	12.6 $\mu$ s	12.6 $\mu$ s
BCALL	C	17.1 $\mu$ s	17.1 $\mu$ s
BLK	C	22.1 $\mu$ s	22.6 $\mu$ s
BEND	None	8.7 $\mu$ s	0 $\mu$ s

## Clock / Calendar Instructions

Clock / Calendar Instructions		DL350	
Instruction	Legal Data Types	Execute	Not Exec
DATE	V:Data Reg.	21.3 $\mu$ s	1.9 $\mu$ s
	V:Bit Reg.	21.3 $\mu$ s	1.9 $\mu$ s
TIME	V:Data Reg.	13.2 $\mu$ s	1.9 $\mu$ s
	V:Bit Reg.	13.2 $\mu$ s	1.9 $\mu$ s

## Drum Instructions

Drum Instructions		DL350	
Instruction	Legal Data Types	Execute	Not Exe.
DRUM	CT	340.0 $\mu$ s	62.6 $\mu$ s
EDRUM	CT	243.0 $\mu$ s	100.0 $\mu$ s
MDRMD	CT	206.0 $\mu$ s	142.00 $\mu$ s
MDRMW	CT	150.0 $\mu$ s	94.00 $\mu$ s