Index

A

ASCII Table, H–2

Auxiliary Functions, 3–8, A–2
- accessing
  - with ***Direct***SOFT, A–3
  - with the Handheld, A–3

B

Bases
- conventional specifications, F–5
- expansion, 4–9, F–8
- installing modules, 2–9, 2–11
- local, 4–9, F–8
- mounting dimensions, 2–10
- power wiring, 2–13
- setting base jumpers, F–10
- setting switches, 4–11, F–10
- Slot Numbering, 2–25
- Specifications, 4–5

Battery
- CPU indicator, 9–2
- replacement, 9–2

I/O Modules, Troubleshooting, 9–13

C

Clock and Calendar, 3–9

Communication
- ports, 3–5
- setting addresses, 3–10

Communications, Problems, 9–12

Configuration
- I/O
  - automatic check, A–5
  - selecting a new configuration, A–5
  - viewing, A–5
  - I/O examples, F–11–F–19

Convergence Stages, 7–19, 7–25

Conventional I/O Numbering, F–2

CPU
- battery, 9–2
- Battery Backup, 3–6
- clearing memory, 3–9, A–4
- Diagnostics, 3–15
- features, 3–2, 3–4
- Indicators, 9–9
- Mode Operation, 3–12
- Mode Switch, 3–4
- Port 1 Specifications, 3–5
- Port 2 Specifications, 3–5
- Scan Time, 3–18
- setup, 3–7
  - clearing memory, 3–9
  - initializing system memory, 3–9
- Specifications, 3–3
- Status Indicators, 3–4

D

Diagnostics, 9–3

Dimensions, 2–10

DirectNET, 4–22
- ***Direct***NET Port Configuration, 4–24
- Network Master Operation, 4–30
- Network Slave Operation, 4–25

Discrete Input, specifications, 2–28–2–39

Discrete Output, specifications, 2–40–2–54

DL405 Aliases, 3–30

Drum instructions, 6–12

Drum sequencers, 6–2

Drum step transitions, 6–4

Duplicate Reference Check, A–4

E

Emergency Stop Switch, 2–3

Error Codes
- fatal, 9–3

listing, B-2–B-9
non-fatal, 9-3
Program, 9-8
special relays assigned to, 9-5
System, 9-7
V-memory locations for, 9-4
European Directives, J-2
Expansion Bases, 4-9, 4-10, & F-8 to F-9

F

Fatal Errors, 9-3, 9-7
Forcing I/O, 3-13, 9-24

G

Grounding, 2-6 to 2-7 & 2-8 to 2-9

I

I/O Modules
address switch (base), 4-11, F-10
configuration, A-5
power up check, A-5
viewing, A-5
configuration history, F-2
diagnostics, A-5
discrete input specifications, 2-28–2-39
discrete output specifications, 2-40–2-54
example configurations, F-11–F-19
numbering, F-2, F-3
placement, 4-3–4-7, F-4–F-6
point requirements, F-3
I/O Modules Wiring, 2-24, 2-26
I/O Response Time, 3-16
I/O Wiring Strategies, 2-14
Initial Stages, 7-5, 7-23
Input Modules
specifications, 2-28–2-39
wiring diagrams, 2-28–2-39
Installation
base, mounting dimensions, 2-10
component dimensions, 2-10
grounding, 2-4–2-5
installing modules, 2-9, 2-11
local and expansion bases, 4-9, F-8
panel design specifications, 2-4
Instruction Set, index table, 5-3
Instructions, 5-2
execution times, C-2–C-23
stage, 7-23
stage programming, 7-2

J

Jump Instruction, 7-7 & 7-24
Jumpers, on bases, F-10
Jumpers, on bases, 4-11

L

Local Bases, 4-9, F-8

M

Masked drums, 6-18
Math Instructions, 5-77
Memory, G-2
clearing, 3-9
program memory, A-4
V-memory, A-4
Control Relay Bit Map, 3-31, 3-33
DL350 Memory Map, 3-29
initializing system memory, 3-9
map, 3-23
Scratch Pad Memory, 3-9
Stage Bit Map, 3-35
X input/Y output map, 3-30, 3-32
MODBUS, 4-22
MODBUS Port Configuration, 4-23
Network Master Operation, 4-30
Network Slave Operation, 4-25
Mode Switch, 3-4
Module Placement, 4-3
Module Power Requirement, 4-5
Mounting
Guidelines, 2-4
Panel, 2-5, 2-7

N

Netork Address, A-6
Network Address, 3-10
Non-fatal Errors, 9-3
Number Conversions, 5-103
Numbering Systems
BCD, I-5
Binary, I-2
Floating Point, I-6
Hexadecimal, I-3
Octal, I-4

O

Output Modules
power disconnect, 2-3
specifications, 2-40–2-54
wiring diagrams, 2-40–2-54

P

Part Numbering Scheme, 1–8

Password Protection, 3–10

PID
- Analog Filter, 8–54
- Bumpless Transfer, 8–13, 8–27
- Cascade Control, 8–63
  - Tuning, 8–65
- Control Introduction, 8–4
- ***Direct***SOFT 5 Filter, 8–55
- DL450 Control, 8–6
- Error Flags, 8–18
- Error Term Selection, 8–33
- Example Program, 8–70
- Loop Modes, 8–28, 8–53
- On/Off Control, 8–66
- Operation, 8–9
- Parameters, 8–32
- PID View, 8–49–8–51
- Ramp/Soak, 8–39
- Reset Windup, 8–10, 8–34
- Special Features, 8–52
- Time Proportioning, 8–66

PID Alarms
- Alarm Features, 8–3
- Auto Tuning Error, 8–48
- Hysteresis, 8–13, 8–36, 8–38
- Monitor Limit, 8–35
- Overflow/Underflow Error, 8–38
- Programming Error, 8–38
- PV Deviation, 8–36
- Rate–of–Change, 8–13, 8–37
- Setup Alarms, 8–35

PID Loop
- Alarms, 8–13
- Configure, 8–26
- Features, 8–2, 8–3
- Feedforward Control, 8–68
- Freeze Bias, 8–11, 8–34
- Loop Definitions, 8–21
- Mode, 8–28
- Operating Modes, 8–14
- Special Loop Calculations, 8–14
- Setup, 8–18
- Terminology, 8–74
- Time–Proportioning Control, On/Off Control Example, 8–67
- Transfer Mode, 8–27
- Troubleshooting Tips, 8–72
- Tuning, 8–40
  - Auto , 8–45
  - Manual, 8–41–8–44

PID Mode 2 Word Description, 8–23

PID Mode Setting 1 Description, 8–22

PID Position Algorithm, 8–9, 8–15
- Position Form, 8–9

PID Velocity Algorithm, 8–9
- Algorithm Form, 8–12
- Velocity Algorithm, 8–15

PLC Numbering System, 3–21

Power Budget, 4–5
- Example, 4–7

Power Indicator, 9–10

Programming
- changing I/O references, A–4
- checking for duplicate references, A–4
- checking the program syntax, A–4
- clearing memory, A–4
- instruction execution times, C–2–C–23
- instruction set index, 5–3

R

Ramp/Soak Generator, 8–56
- Controls, 8–59
- ***Direct***SOFT Example, 8–61
- Flag Bit Description Table, 8–24
- Profile Monitoring, 8–60
- Table, 8–57
- Table Flags, 8–59
- Table Location, 8–25
- Test the Profile, 8–62
- Testing, 8–60

Remote I/O
- Port Connections, 4–18
- Remote I/O Expansion, 4–16

Retentive Memory, 3–10

RLL^{PLUS}, instructions, 7–23–7–29

Run Relay, F–7

Run Time Edits, 9–22

S

Safety
- emergency switch, 2–3
- guidelines, 2–2–2–3
- levels of protection, 2–2
- output module power disconnect, 2–3
- panel design specifications, 2–4
- planning for, 2–2
- sources of assistance, 2–2

Scan Time, 3–18

Sinking/Sourcing, 2–17

Special Relays, 9–5

Specifications
- component weights, E–2

discrete input modules, 2–28–2–39
discrete output modules, 2–40–2–54
panel design, 2–4
Stage Counter instruction, 7–16
Stage programming, 7–2
convergence, 7–19
four steps to writing a stage program, 7–9
garage door opener example, 7–10
initial stages, 7–5
instructions, 7–23–7–29
introduction, 7–2
jump instruction, 7–7
managing large programs, 7–21
mutually exclusive transitions, 7–14
parallel processes, 7–12
parallel processing concepts, 7–19
power flow transition, 7–18
program organization, 7–15
questions and answers, 7–29
stage view, 7–28
state transition diagrams, 7–3
supervisor process, 7–17
timer inside stage, 7–13
unconditional outputs, 7–18
Stages, blocks, 7–27
System
component dimensions, 2–10
memory initialization, 3–9
panel design specifications, 2–4
V–Memory, 3–27
System design strategies, 4–2

T

Timed drum, 6–12
Troubleshooting, 9–16
cabinet air environment, 9–2
error codes, B–2
special relays for, 9–5
V–memory locations for, 9–4
fatal errors, 9–3
finding diagnostic information, 9–3
I/O modules, A–5
selecting a new configuration, A–5
low battery, 9–2
machine startup and program, 9–17
non–fatal errors, 9–3

W

Watchdog Timer, A–6
Wiring, base power supply, 2–13

V

Velocity algorithm, 8–30

W

Watchdog Timer, A–6
Wiring, base power supply, 2–11