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DL305 Data Types and Memory Map

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DL305 Data Types

The following table shows the data types available with the DL405 family of products.

DL305 Data Type	Description	Bits per unit	Number of bytes	
			HEX	ASCII
31	Data registers	8	1	2
	T / C accumulator	16	2	4
33	I/O, internal relays, shift register bits, T/C bits, stage bits	1	1	2
39	Diagnostic Status (5 word R/W)	16	10	20

Data Types 31 and 33

The following table provides address references for data types 31 and 33.

DL305 Data Type	Description	Read/ Write	DL330 Ranges		DL340 Ranges	
			PGM Ref.	*Direct*NET Ref	PGM Ref.	*Direct*NET Ref
31	Data registers	R / W	400 – 577	41 – 80	400 – 577	41 – 80
					700 – 777	81 – A0
	T / C accumulator		600 – 677	01 – 40	01 – 40	01 – 40
33	Input / Output bits	R/W	000 – 157	01 – 0E	000 – 157	01 – 0E
		R/W	700 – 767	39 – 3F	700 – 767	39 – 3F
		R/W			1000–1067	41 – 47
	Internal Relay Bits	Read	160 – 377	0F – 20	160 – 377	0F – 20
		Write	160 – 373	0F – 20	160 – 373	0F – 20
	Shift Register Bits	R / W	400 – 577	21 – 30	400 – 577	21 – 30
	T / C Bits	Read	600 – 677	31 – 38	600 – 677	31 – 38

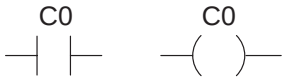
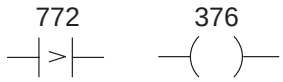
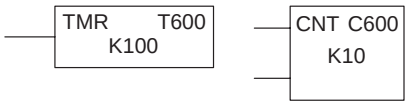
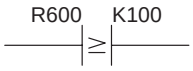
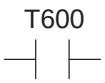
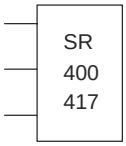
Data Type 39 Diagnostic Status

You can use Data Type 39 to obtain ***Direct***NET diagnostic status. The only valid address for the DL305 products is 0000 (hex). There are 5 status words that can be read or cleared. You must access these words as a complete group. The following tables show the reference addresses for the various types of information and the ***Direct***NET error codes (used for word 1).

Address	Read/Write	Word	Diagnostic Status
0000 (h)	Read Write 0 (to clear)	1	Last error and previous error* Previous error code
		2	Number of successful communications
		3	Number of erroneous communications
		4	Number of retries for header
		5	Number of retries for data
* The last error code is contained in the most significant byte. The previous error code is in the least significant byte. Two codes that are displayed are cleared by two successful communication exchanges.			

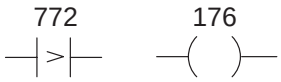
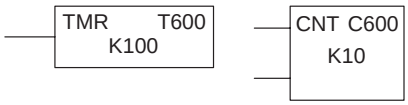
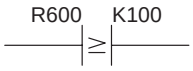
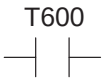
Error Code	Applicable Data Type	Error Description
00	All types	The transfer was successful. 00 also occurs if: 1. The transfer direction (Read / Write) is not 30 or 38. 2. A code other than ASCII code 0 to F has been received in ASCII mode. 3. E01 or E10 occurred during a write operation from the host to the CPU.
01	All types	A timeout occurred in the serial link.
03	32, 33	A request was made to read or write a non-existent I/O point.
04	32, 33	A request was made for data of more I/O points than are available.
05	All types	A request was made to read or write odd bytes. The number of data requested was not a multiple of 4 in the ASCII mode.
06	31	A request was made to read or write one or more non-existent memory locations.
07	All types	A request was made to read or write a zero data byte.
08	36	An attempt was made to write a protected memory.
09	All types	An invalid code is specified or an attempt was made to write to an invalid address.
0A	39	A request was made to read or write one or more non-existent diagnostic status words.
0B	36, 39	An invalid starting address is used in the PC type read, scan start/stop, diagnostic status read or write request.
0C	All types	Three attempts were made to transmit the header.
0D	All types	Three attempts were made to transmit the data.
0F	All types	The header unit number is incorrect. An invalid function was requested.
10	All types	Power is turned on
	31, 33	After power-up, an attempt was made to execute a function before a scan start/stop, or diagnostic status read or write.
14	All types	One or more errors occurred during the data block transfer. Possible errors are: invalid STX, ETC, LRC, or ETB is received; a parity, framing, or overrun error occurred.
15	All types	EOT from the master station could not be received.
16	All types	A code other than ACK or NAK was received.
1D	31, 33	In the data transfer between the host and the slave, one of the following errors occurred in the slave CPU: E02, E21, E31, or E41.
	36	The communication between the host and the slave is disconnected.
1E	All types	There is a format error in the header block.

DL330 Memory Map

Memory Type	Discrete Memory Reference (octal)	Register Memory Reference (octal)	Qty. Decimal	Symbol
Input / Output Points	000 – 157 700 – 767	R000 – R015 R070 – R076	168 Total	
Control Relays	160 – 373	R016 – R037	140	
Special Relays	374 – 377 770 – 777	R037 R077	12	
Timers / Counters	600 – 673 674 – 677*	None	64	
Timer / Counter Current Values	None	R600 – R673 R674 – R677*	64	
Timer / Counter Status Bits	T600 – T673 T674 – T677*	None	64	
Data Words	None	R400 – R563	116	None specific, used with many instructions
Shift Registers	400 – 577	None	128	
Special Registers	None	R574 – R577	4	R574 – R575 used with FAULT R576 – R577 Auxiliary Accumulator

* T/ C Setpoint Unit Only. Can be used as data registers if the Timer/Counter Setpoint Unit or Thumbwheel Interface Module is not used. R564 – R573 contain the preset value used with the Timer / Counter Setpoint Unit. R674 – R677 contain the current values for these timers or counters.

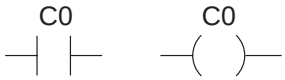
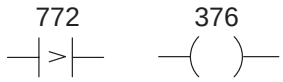
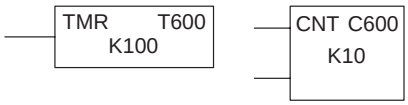
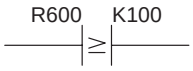
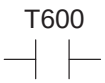
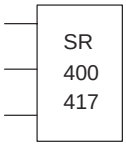
DL330P Memory Map

Memory Type	Discrete Memory Reference (octal)	Register Memory Reference (octal)	Qty. Decimal	Symbol
Input / Output Points	000 – 157 700 – 767	R000 – R015 R070 – R076	168 Total	
Control Relays	160 – 174 200 – 277	R016 – R017 R020 – R027	77	
Special Relays	175 – 177 770 – 777	R017 R077	11	
Timers / Counters	600 – 673 674 – 677*	None	64	
Timer / Counter Current Values	None	R600 – R673 R674 – R677*	64	
Timer / Counter Status Bits	T600 – T673 T674 – T677*	None	64	
Data Words	None	R400 – R563	116	None specific, used with many instructions
Stages	S0 – S177	R100 – R117	128	
Special Registers	None	R574 – R577	4	R574 – R575 used with FAULT R576 – R577 Auxiliary Accumulator

* T/ C Setpoint Unit Only. Can be used as data registers if the Timer/Counter Setpoint Unit or Thumbwheel Interface Module is not used, which provides a total of 128 data registers.

R564 – R573 contain the preset value used with the Timer / Counter Setpoint Unit. R674 – R677 contain the current values for these timers or counters.

DL340 Memory Map

Memory Type	Discrete Memory Reference (octal)	Register Memory Reference (octal)	Qty. Decimal	Symbol
Input / Output Points	000 – 157 700 – 767	R000 – R015 R070 – R076	168 Total	
Control Relays	160 – 373 1000 – 1067	R016 – R037 R100 – R106	180	
Special Relays	374 – 377 770 – 777 1070 – 1077	R037 R077 R107	20	
Timers / Counters	600 – 673 674 – 677*	None	64	
Timer / Counter Current Values	None	R600 – R673 R674 – R677*	64	
Timer / Counter Status Bits	T600 – T673 T674 – T677*	None	64	
Data Words	None	R400 – R563 R700 – R767	172	None specific, used with many instructions
Shift Registers	400 – 577	None	128	
Special Registers	None	R574 – R577 R770 – R777	12	R574–R575 used with FAULT R576–R577 Auxiliary Accumulator R770–R777 Communications Setup

* T/ C Setpoint Unit Only. Can be used as data registers if the Timer/Counter Setpoint Unit or Thumbwheel Interface Module is not used. R564 – R573 contain the preset value used with the Timer / Counter Setpoint Unit. R674 – R677 contain the current values for these timers or counters.

I/O Point Bit Map

These tables provide a listing of the individual Input points associated with each register location for the DL330, DL330P, and DL340 CPUs.

MSB			I/O References				LSB	Register Number
007	006	005	004	003	002	001	000	R0
017	016	015	014	013	012	011	010	R1
027	026	025	024	023	022	021	020	R2
037	036	035	034	033	032	031	030	R3
047	046	045	044	043	042	041	040	R4
057	056	055	054	053	052	051	050	R5
067	066	065	064	063	062	061	060	R6
077	076	075	074	073	072	071	070	R7
107	106	105	104	103	102	101	100	R10
117	116	115	114	113	112	111	110	R11
127	126	125	124	123	122	121	120	R12
137	136	135	134	133	132	131	130	R13
147	146	145	144	143	142	141	140	R14
157	156	155	154	153	152	151	150	R15
167	166	165	164	163	162	161	160	n/a
177	176	175	174	173	172	171	170	n/a
707	706	705	704	703	702	701	700	R70
717	716	715	714	713	712	711	710	R71
727	726	725	724	723	722	721	720	R72
737	736	735	734	733	732	731	730	R73
747	746	745	744	743	742	741	740	R74
757	756	755	754	753	752	751	750	R75
767	766	765	764	763	762	761	760	R76

NOTE: 160 – 167 can be used as I/O in a DL330 or DL330P CPU under certain conditions. 160 – 177 can be used as I/O in a DL340 CPU under certain conditions. You should consult the DL305 User Manual to determine which configurations allow the use of these points.

These points may be used as control relays. You cannot use them as both control relays and as I/O points. Also, if you use these points as I/O, you cannot access these I/O points as a Data Register reference using the DSTR5 (F55) and DOUT5 (F65) functions.

Control Relay Bit Map

The following tables provide a listing of the individual control relays associated with each register location for the DL305 CPUs.

NOTE: 160 – 167 can be used as I/O in a DL330 or DL330P CPU under certain conditions. 160 – 177 can be used as I/O in a DL340 CPU under certain conditions. You should consult the DL305 User Manual to determine which configurations allow the use of these points.

You cannot use them as both control relays and as I/O points. Also, if you use these points as I/O, you cannot access these I/O points as a Data Register reference using the DSTR5 (F55) and DOUT5 (F65) functions.

MSB			DL330 Control Relay References				LSB	Register Number
167	166	165	164	163	162	161	160	R16
177	176	175	174	173	172	171	170	R17
207	206	205	204	203	202	201	200	R20
217	216	215	214	213	212	211	210	R21
227	226	225	224	223	222	221	220	R22
237	236	235	234	233	232	231	230	R23
247	246	245	244	243	242	241	240	R24
257	256	255	254	253	252	251	250	R25
267	266	265	264	263	262	261	260	R26
277	276	275	274	273	272	271	270	R27
307	306	305	304	303	302	301	300	R30
317	316	315	314	313	312	311	310	R31
327	326	325	324	323	322	321	320	R32
337	336	335	334	333	332	331	330	R33
347	346	345	344	343	342	341	340	R34
357	356	355	354	353	352	351	350	R35
367	366	365	364	363	362	361	360	R36
				373	372	371	370	R37

* Control relays 340 – 373 can be made retentive by setting a CPU dipswitch. See the DL305 User Manual for details on setting CPU dipswitches.

MSB			DL330P Control Relay References				LSB	Register Number
167	166	165	164	163	162	161	160	R16
			174	173	172	171	170	R17
207	206	205	204	203	202	201	200*	R20
217	216	215	214	213	212	211	210	R21
227	226	225	224	223	222	221	220	R22
237	236	235	234	233	232	231	230	R23
247	246	245	244	243	242	241	240	R24
257	256	255	254	253	252	251	250	R25
267	266	265	264	263	262	261	260	R26
277*	276	275	274	273	272	271	270	R27

* Control relays 200 – 277 can be made retentive by setting a CPU dipswitch. See the DL305 User Manual for details on setting CPU dipswitches.

MSB			DL340 Control Relay References				LSB	Register Number
167	166	165	164	163	162	161	160	R16
177	176	175	174	173	172	171	170	R17
207	206	205	204	203	202	201	200	R20
217	216	215	214	213	212	211	210	R21
227	226	225	224	223	222	221	220	R22
237	236	235	234	233	232	231	230	R23
247	246	245	244	243	242	241	240	R24
257	256	255	254	253	252	251	250	R25
267	266	265	264	263	262	261	260	R26
277	276	275	274	273	272	271	270	R27
307	306	305	304	303	302	301	300	R30
317	316	315	314	313	312	311	310	R31
327	326	325	324	323	322	321	320	R32
337	336	335	334	333	332	331	330	R33
347	346	345	344	343	342	341	340*	R34
357	356	355	354	353	352	351	350	R35
367	366	365	364	363	362	361	360	R36
				373*	372	371	370	R37
1007	1006	1005	1004	1003	1002	1001	1000	R100
1017	1016	1015	1014	1013	1012	1011	1010	R101
1027	1026	1025	1024	1023	1022	1021	1020	R102
1037	1036	1035	1034	1033	1032	1031	1030	R103
1047	1046	1045	1044	1043	1042	1041	1040	R104
1057	1056	1055	1054	1053	1052	1051	1050	R105
1067	1066	1065	1064	1063	1062	1061	1060	R106

* Control relays 340 – 373 can be made retentive by setting a CPU dipswitch. See the DL305 User Manual for details on setting CPU dipswitches.

Special Relays

The following table shows the Special Relays used with the DL305 CPUs.

CPUs	Special Relay	Description of Contents
DL330P	175	100 ms clock, on for 50 ms and off for 50 ms.
	176	Disables all outputs except for those entered with the SET OUT instruction.
	177	Battery voltage is low.
DL330 DL340	374	On for the first scan cycle after the CPU is switched to Run Mode.
	375	100 ms clock, on for 50 ms and off for 50 ms.
	376	Disables all outputs except for those entered with the SET OUT instruction.
	377	Battery voltage is low.
DL330 DL330P DL340	770	Changes timers to 0.01 second intervals. Timers are normally 0.1 second time intervals.
	771	The external diagnostics FAULT instruction (F20) is in use.
	772	The data in the accumulator is greater than the comparison value.
	773	The data in the accumulator is equal to the comparison value.
	774	The data in the accumulator is less than the comparison value.
	775	An accumulator carry or borrow condition has occurred.
	776	The accumulator value is zero.
	777	The accumulator has an overflow condition.
DL340	1074	The RX or WX instruction is active.
	1075	An error occurred during communications with the RX or WX instructions.
	1076	Port 2 communications mode: on = ASCII mode, off = HEX mode. ***Direct***NET supports both ASCII and HEX modes and Modbus® only supports HEX mode.
	1077	Port 1 communications mode: on = ASCII mode, off = HEX mode

Timer / Counter Registers and Contacts

The following table shows the locations used for programming timer or counters. Since timers and counters share the same data area, you cannot have timers and counters with duplicate numbers. For example, if you have Timer 600, you cannot have a Counter 600.
Each register contains the current value for the timer or counter. Each timer or counter also has a timer or counter contact with the same reference number.

NOTE: Counter current values are retentive and retain their state after a power cycle.

Timer/Counter References/Registers							
607	606	605	604	603	602	601	600
617	616	615	614	613	612	611	610
627	626	625	624	623	622	621	620
637	636	635	634	633	632	631	630
647	646	645	644	643	642	641	640
657	656	655	654	653	652	651	650
667	666	665	664	663	662	661	660
677*	676*	675*	674*	673	672	671	670

* Used with Timer / Counter Setpoint Unit and /or Thumbwheel Interface Module.

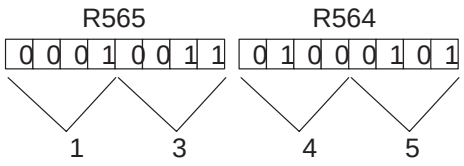
External Timer/Counter Setpoint Unit

Registers 674–677 are used in programming for use with the Timer/Counter Setpoint Unit and the Thumbwheel Interface Module that are available in some compatible product families. The registers contain the current time or count. There is also a status bit for each register with the same reference number. For example, the current value for Timer 674 is stored in R674 and the status contact is T674.

The presets for these modules are stored in R564 – R573 as follows.

- R564 – R565 — 1st T/C preset
- R566 – R567 — 2nd T/C preset
- R570 – R571 — 3rd T/C preset
- R572 – R573 — 4th T/C preset

The example shows how a 4-digit number would be represented in these registers.



Data Registers

The following 8-bit data registers are primarily used with data instructions to store various types of application data. For example, you could use a register to hold a timer or counter preset value.

Some data instructions call for two bytes, which will correspond to two consecutive 8-bit data registers such as R401 and R400. The LSB (Least Significant Bit) will be in register R400 as bit0 and the MSB (Most Significant Bit) will be in register R401 as bit17.

NOTE: Data Registers are retentive.

DL330 / DL330P 8-Bit Data Registers							
407	406	405	404	403	402	401	400
417	416	415	414	413	412	411	410
427	426	425	424	423	422	421	420
437	436	435	434	433	432	431	430
447	446	445	444	443	442	441	440
457	456	455	454	453	452	451	450
467	466	465	464	463	462	461	460
477	476	475	474	473	472	471	470
507	506	505	504	503	502	501	500
517	516	515	514	513	512	511	510
527	526	525	524	523	522	521	520
537	536	535	534	533	532	531	530
547	546	545	544	543	542	541	540
557	556	555	554	553	552	551	550
				563	562	561	560

DL340 8-Bit Data Registers							
407	406	405	404	403	402	401	400
417	416	415	414	413	412	411	410
427	426	425	424	423	422	421	420
437	436	435	434	433	432	431	430
447	446	445	444	443	442	441	440
457	456	455	454	453	452	451	450
467	466	465	464	463	462	461	460
477	476	475	474	473	472	471	470
507	506	505	504	503	502	501	500
517	516	515	514	513	512	511	510
527	526	525	524	523	522	521	520
537	536	535	534	533	532	531	530
547	546	545	544	543	542	541	540
557	556	555	554	553	552	551	550
				563	562	561	560
707	706	705	704	703	702	701	700
717	716	715	714	713	712	711	710
727	726	725	724	723	722	721	720
737	736	735	734	733	732	731	730
747	746	745	744	743	742	741	740
757	756	755	754	753	752	751	750
767	766	765	764	763	762	761	760

Stage Control / Status Bit Map

This table provides a listing of the individual stages and stage control bits. These are only available with the DL330P CPU.

MSB			Stage References				LSB	Register Number
007	006	005	004	003	002	001	000	R100
017	016	015	014	013	012	011	010	R101
027	026	025	024	023	022	021	020	R102
037	036	035	034	033	032	031	030	R103
047	046	045	044	043	042	041	040	R104
057	056	055	054	053	052	051	050	R105
067	066	065	064	063	062	061	060	R106
077	076	075	074	073	072	071	070	R107
107	106	105	104	103	102	101	100	R110
117	116	115	114	113	112	111	110	R111
127	126	125	124	123	122	121	120	R112
137	136	135	134	133	132	131	130	R113
147	146	145	144	143	142	141	140	R114
157	156	155	154	153	152	151	150	R115
167	166	165	164	163	162	161	160	R116
177	176	175	174	173	172	171	170	R117

Shift Register Bit Map

The shift register bits listed below are used in the shift register instruction. These outputs are discrete bits and are not the same locations as the 8 Bit Data Registers. These bits are retentive meaning they retain their state after a power cycle.

NOTE: The DL330P does not have Shift Register bits. Shift Register instructions in the DL330P use Control Relays memory references.

MSB			DL330 / DL340 Shift Register References				LSB	Register Number
407	406	405	404	403	402	401	400	R40
417	416	415	414	413	412	411	410	R41
427	426	425	424	423	422	421	420	R42
437	436	435	434	433	432	431	430	R43
447	446	445	444	443	442	441	440	R44
457	456	455	454	453	452	451	450	R45
467	466	465	464	463	462	461	460	R46
477	476	475	474	473	472	471	470	R47
507	506	505	504	503	502	501	500	R50
517	516	515	514	513	512	511	510	R51
527	526	525	524	523	522	521	520	R52
537	536	535	534	533	532	531	530	R53
547	546	545	544	543	542	541	540	R54
557	556	555	554	553	552	551	550	R55
567	566	565	564	563	562	561	560	R56
577	576	575	574	573	572	571	570	R57

With the DL340 CPU, these bits can also be used as control relays if they are not used with a Shift Register instruction.

Special Registers

This table provides a listing of the special registers used with the DL305 CPUs.

CPUs	Special Register	Description of Contents
DL330 DL330P DL340	R574 – 575	Contains the error code used with the FAULT instruction.
	R576 – 577	Auxiliary accumulator used with the MUL and DIV instructions.
DL340 Only	R771	Sets the upper byte of the station address assigned to the bottom communication port. Therefore, this will contain the 1st and 2nd digits of the address.
	R772	Sets the lower byte of the station address assigned to the bottom communication port. This only contains one digit, which is the 3rd digit of the address.
	R773	Sets the baud rate for the bottom communication port.
	R774	Sets the leading communications delay time for the bottom communication port.
	R775	Sets the trailing communications delay time for the bottom communication port.
	R776	Sets the leading communications delay time for the top communication port.
	R777	Sets the trailing communications delay time for the top communication port.

DL305 / 405 Cross Reference

If you are using a DL405 Master, you will have to make some slight changes in the way you request certain types of data. For example, the DL405 uses V-memory references instead of Register references. This section shows the cross references.

NOTE: Not all DL305 devices offer the same memory ranges. Check your DL305 User Manual to determine the ranges for your particular model.

Data Type 31: Register Access

To get to ... TMR / CTR Accumulator in a DL305	Use Reference ... in a DL405	To get to ... Register Data in a DL305	Use Reference ... in a DL405
R600	V000	R401, 400*	V100
R601	V001	R403, 402	V101
— — —	— — —	— — —	— — —
R624	V024	R777, 776	V237
R677	V077		
Two bytes of DL305 register data are returned with one DL405 V memory location.			

Data Type 33: I/O Point Access

Non RLL*PLUS* CPUs			
To get to ... I/O Points, CRs, & Shift Registers in a DL305	**Use Reference ... in a DL405**	**To get to ... TMR / CNT Status Bit in a DL305**	**Use Reference ... in a DL405**
IO 000	GY000	600	GY600
IO 001	GY001	601	GY601
— — —	— — —	— — —	— — —
IO 157	GY157	677	GY677
CR160	GY160		
— — —	— — —		
CR 377	GY377		
IO 700	GY700		
IO 701	GY701		
— — —	— — —		
IO 1067	GY1067		
SR 400	GY400		
SR 401	GY401		
— — —	— — —		
SR 577	GY577		

RLL*PLUS* CPUs					
To get to ... I/O Points, CRs, & Shift Registers in a DL305	**Use Ref. ... in a DL405**	**To get to ... Stage Status Bit in a DL305**	**Use Ref. ... in a DL405**	**To get to ... TMR / CNT Status Bit in a DL305**	**Use Ref. ... in a DL405**
IO 000	GY000	000	GY200	600	GY600
IO 001	GY001	001	GY201	601	GY601
— — —	— — —	— — —	— — —	— — —	— — —
CR160	GY160	177	GY377	677	GY677
— — —	— — —				
CR 277	GY277				
IO 700	GY700				
IO 701	GY701				
IO 1067	GY1067				
SR 200	GY400				
SR 201	GY 401				
— — —	— — —				
SR 277	GY477				