Memory Mapping

In This Appendix...

Input Memory Map for Data Transfers from CTRIO(2) to DL CPUs

☑ DL
☑ Win
☑ NI

The following table shows which memory locations are used for memory transfers from the CTRIO(2) module to the CPU. The starting memory location is defined by the user in the I/O Map within CTRIO Workbench. If you are using the *Direct*LOGIC CPU, you will use the memory address offsets in the second column. If using an H2-WinPLC, EBC, PBC, MODBUS, or DEVNETS in the CPU slot, you will use the non-PLC offsets in column one.

Data Type and Offset WinPLC, EBC, PBC, DEVNETS, MODBUS	Address for Inputs (*Direct*LOGIC)	Definition	Format	Bytes
dwX0	n+0	Ch 1/Fn 1 Parameter 1	DWord	4
dwX1	n+2	Ch 1/Fn 1 Parameter 2		
dwX2	n+4	Ch 1/Fn 2 Parameter 1		
dwX3	n+6	Ch 1/Fn 2 Parameter 2		
dwX4	n+10	Ch 2/Fn 1 Parameter 1		
dwX5	n+12	Ch 2/Fn 1 Parameter 2		
dwX6	n+14	Ch 2/Fn 2 Parameter 1		
dwX7	n+16	Ch 2/Fn 2 Parameter 2		
bX0...7 bX8...15	n+20	Ch 1/Fn 1 Status (Low Byte) Ch 1/Fn 2 Status (High Byte)	Word	2
bX16...23 bX24...31	n+21	Ch 2/Fn 1 Status (Low Byte) Ch 2/Fn 2 Status (High Byte)		
bX32...39 bX40...47	n+22	Output 0 Status (Low Byte) Output 1 Status (High Byte)		
bX48...55 bX56...63	n+23	Output 2 Status (Low Byte) Output 3 Status (High Byte)		
bX64...71 bX72...79 bX80...87 bX88...95	n+24	System Functions Read/Write CTRIO(2) Internal Registers (see p. 6-10 for bit definitions)	DWord	4
				44 Total Bytes

Input (n) Parameter Definitions

Parameter values are in Decimal format.

Configured Function from CTRIO Workbench	Parameter 1 Contents DWORD	Parameter 2 Contents DWORD
Non-scaled Counter	Raw Input Value	Not Used
Scaled Counter	Scaled Value (pos. or rate)	Raw Value
Non-scaled Counter with Capture	Raw Value	Captured Value
Scaled Counter with Capture	Scaled Value (pos. or rate)	Scaled Captured Value
Non-scaled Timer	Previous Time (µs)	In Progress Time (µs)
Scaled Timer	Scaled Interval (rate)	Scaled In Progress Time (µs)
Pulse Catch	Not Used	Not Used

NOTE: *For* ***Direct****SOFT users: the* ***I/O Map*** *dialog displays the exact memory locations in use by the CTRIO(2) module. Within the I/O Map dialog you can print out a report of memory loctions in use.*

Input Function Status Bit Definitions

Input function offsets are listed in the order of Ch1/Fn1, Ch1/Fn2, Ch2/Fn1, Ch2/Fn2

Ch(x)/Fn(x) Status Bits (Transfers from CTRIO(2) to CPU)	Bit Offsets: WinPLC, EBC, PBC, DEVNETS, MODBUS	V-memory Offsets *Direct*LOGIC PLCs
Count Capture Complete Bit	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8
Timer Capture Start	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8
Timer Capture Complete (Timing) OR At Reset Value (Counting)	1, 9, 17, 25	20.1, 20.9, 21.1, 21.9
Timer "Timed Out" Bit	2, 10, 18, 26	20.2, 20.10, 21.2, 21.10
Pulse Catch Output Pulse State	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8
Pulse Catch Start	1, 9, 17, 25	20.1, 20.9, 21.1, 21.9

Output Status Bit Definitions (for Preset Table Control)

Output Status Offsets are listed in the order of the Output 0 - Output 3.

Output(x) Status Bits (Transfers from CTRIO(2) to CPU)	Bit Offsets: WinPLC, EBC, PBC, DEVNETS, MODBUS	V-memory Offsets *Direct*LOGIC PLCs
Command Error	38, 46, 54, 62	22.6, 22.14, 23.6, 23.14
Command Complete	39, 47, 55, 63	22.7, 22.15, 23.7, 23.15

Output Status Bit Definitions (Pulse Output)

Output Status Offsets are listed in the order of the Output 0/1, 2/3.

Status Bit CTRIO(2) to CPU	Bit Offsets: WinPLC, EBC, PBC, DEVNETS, MODBUS	V-memory Offsets from Input Start (octal)
Output Enabled	32, 48	22.0, 23.0
Position Loaded	33, 49	22.1, 23.1
Output Suspended	34, 50	22.2, 23.2
Output Active	36, 52	22.4, 23.4
Output Stalled	37, 53	22.5, 23.5
Command Error	38, 54	22.6, 23.6
Command Complete	39, 55	22.7, 23.7

Output Memory Map for Data Transfers from DL CPUs to CTRIO(2)

☑ DL
☑ Win
☑ NI

The following table shows which memory locations are used for memory transfers from the CPU module to the CTRIO(2). The starting memory location is defined by the user in the I/O Map within CTRIO Workbench. If you are using a *Direct*LOGIC CPU, you will use the memory address offsets in the second column. If you are using a WinPLC, EBC, PBC, DEVNETS or MODBUS interface, you will use the non-PLC offsets in column one.

Data Type and Offset: WinPLC, EBC, PBC, DEVNETS, MODBUS	Address for Inputs (*Direct*LOGIC)	Definition	Format	Bytes
dwY0	n+0	Output 0 Parameter 3	DWord	4
dwY1	n+2	Output 1 Parameter 3		
dwY2	n+4	Output 2 Parameter 3		
dwY3	n+6	Output 3 Parameter 3		
wY0	n+10	Output 0 Command	Word	2
wY1	n+11	Output 0 Parameter 1		
wY2	n+12	Output 0 Parameter 2		
wY3	n+13	Output 1 Command		
wY4	n+14	Output 1 Parameter 1		
wY5	n+15	Output 1 Parameter 2		
wY6	n+16	Output 2 Command		
wY7	n+17	Output 2 Parameter 1		
wY8	n+20	Output 2 Parameter 2		
wY9	n+21	Output 3 Command		
wY10	n+22	Output 3 Parameter 1		
wY11	n+23	Output 3 Parameter 2		
bY0...7 bY8...15	n+24	Ch 1/Fn 1 Control (Low Byte) Ch 1/Fn 2 Control (High Byte)	Word	2
bY16...23 bY24...31	n+25	Ch 2/Fn 1 Control (Low Byte) Ch 2/Fn 2 Control (High Byte)		
bY32...39 bY40...47	n+26	Output 0 Control (Low Byte) Output 1 Control (High Byte)		
bY48...55 bY56...63	n+27	Output 2 Control (Low Byte) Output 3 Control (High Byte)		
bY64...71 bY72...79 bY80...87 bY88...95	n+30	System Functions Read/Write CTRIO(2) Internal Registers (see p. 6-10 for bit definitions)	DWord	4

52 Total Bytes

Output (n) Parameter Definitions (Parameters are in decimal format)

Configured Profile from CTRIO Workbench	Parameter 1 Contents WORD	Parameter 2 Contents WORD	Parameter 3 Contents DWORD
Trapezoid /Trapezoid with Limits	File # of stored profile	Not Used	Not Used
S-Curve, Symmetrical S-Curve	File # of stored profile	Not Used	Not Used
Dynamic Positioning /Positioning Plus	File # of stored profile	Not Used	Target Position

Configured Profile from CTRIO Workbench	Parameter 1 Contents WORD	Parameter 2 Contents WORD	Parameter 3 Contents DWORD
Dynamic Velocity	File # of stored profile	Not Used	Target Velocity
Home Search	File # of stored profile	Not Used	Not Used
Trapezoid Plus	File # of stored profile	Not Used	Target Position
Free Form	File # of stored profile	Not Used	Not Used

NOTE: *For* ***Direct****SOFT users: the I/O Map dialog displays the exact memory locations in use by the CTRIO module. Within the I/O Map dialog you can print out a report of memory locations in use.*

Output (n) Parameter Definitions (Parameters are in decimal format unless specified)

Profiles Completely Controlled by User Program	Parameter 1 Contents WORD	Parameter 2 Contents WORD	Parameter 3 Contents DWORD
Velocity Mode	Initial Frequency	Duty Cycle	Number of Pulses (Hex)
Run to Limit Mode	Initial Frequency	Input Edge / Duty Cycle(Hex)	Not Used
Run to Position mode	Initial Frequency	Input Function Comparison and Duty Cycle (Hex)	Input Function Comparison Value

Input Function Control Bit Definitions

Input function offsets are listed in the order of Ch1/Fn1, Ch1/Fn2, Ch2/Fn1, Ch2/Fn2

Ch(n)/Fn(n) Control Bits (Transfers from CPU to CTRIO)	Bit Offsets: WinPLC, EBC, PBC, DEVNETS, MODBUS	V-memory Offsets *Direct*LOGIC PLCs
Enable Count Capture	0, 8, 16, 24	24.0, 24.8, 25.0, 25.8
Enable Timer Capture	0, 8, 16, 24	24.0, 24.8, 25.0, 25.8
Enable Pulse Catch	0, 8, 16, 24	24.0, 24.8, 25.0, 25.8
Reset	1, 9, 17, 25	24.1, 24.9, 25.1, 25.9

Output Control Bit Definitions (for Preset Table Control)

Output Control Offsets are listed in the order of the Output 0 - Output 3.

Output(n) Control Bits (Transfers from CPU to CTRIO(2))	Bit Offsets: WinPLC, EBC, PBC, DEVNETS, MODBUS	V-memory Offsets *Direct*LOGIC PLCs
Enable Output	32, 40, 48, 56	26.0, 26.8, 27.0, 27.8
Process Command	39, 47, 55, 63	26.7, 26.15, 27.7, 27.15

Output Control Bit Definitions (Pulse Output)

Pulse output control Offsets are listed in the order of Outputs 0/1, 2/3.

Output Control Bit (Transfers from CPU to CTRIO(2))	Bit Offsets: WinPLC, EBC, PBC, DEVNETS, MODBUS	V-memory Offsets from Output Start (octal)	Read as:
Enable Output	32, 48	26.0, 27.0	Level
Go to Position	33, 49	26.1, 27.1	Rising Edge
Suspend Output	34, 50	26.2, 27.2	Level
Direction	36, 52	26.4, 27.4	Level
Process Command	39, 55	26.7, 27.7	Rising Edge

Output Control Bit Definitions (Raw Mode)

Output Control Offsets are listed in the order of the Output 0 - Output 3.

Output(n) Control Bits (Transfers from CPU to CTRIO(2))	Bit Offsets: WinPLC, EBC, PBC, DEVNETS, MODBUS	V-memory Offsets DirectLOGIC PLCs
Enable Output	32, 40, 48, 56	26.0, 26.8, 27.0, 27.8

System Functions Status Bit Definitions

*Direct*LOGIC Offset (n+24)

Status Bits (Transfers from CTRIO(2) to CPU)	V-memory Offsets *Direct*LOGIC PLCs
System Command Error	24.6
System Command Complete	24.7
Ch1 A	25.0
Ch1 B	25.1
Ch1 C	25.2
Ch1 D	25.3
Ch2 A	25.4
Ch2 B	25.5
Ch2 C	25.6
Ch2 D	25.7
Out 0 Active	25.8
Out 0 Mode	25.9
Out 1 Active	25.10
Out 1 Mode	25.11
Out 2 Active	25.12
Out 2 Mode	25.13
Out 3 Active	25.14
Out 3 Mode	25.15

System Functions Control Bit Definitions

*Direct*LOGIC Offset (n+30)

Control Bits (Transfers from CPU to CTRIO(2))	V-memory Offsets *Direct*LOGIC PLCs
Process System Command	30.7

Addressing Conventions (with V-memory Examples for DirectLOGIC PLCs)

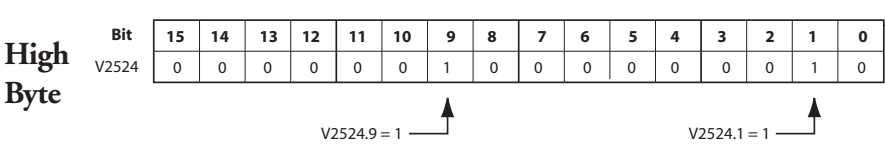
ample for Bit-accessed Data in PLC CPUs

☑ DL ☒ Win ☒ NI

In this example, the V-memory location V2524 contains a value equal to 514 in decimal.

- 514 decimal = 0202 Hex = 0000 0010 0000 0010 binary

The bit V2524.1 refers to the 2nd to the least significant bit (set to 1 in this example). Likewise, V2524.9 refers to bit number 9, the 10th from the least significant bit (also set to 1 in this example).



High Byte and Low Byte of Word Parameters

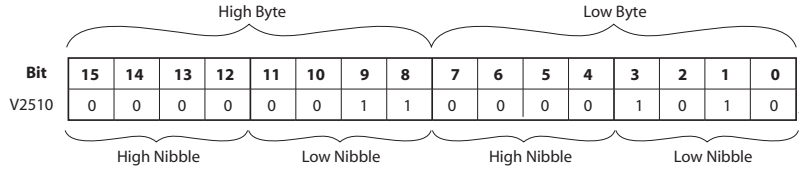
In the following example, the V-memory location V2510 contains a value equal to 3 (decimal) in the high byte and 10 (decimal) in the low byte.

- 3 decimal = 03 Hex = 0000 0011 binary in the high byte, and
- 10 decimal = 0A Hex = 0000 1010 binary in the low byte.

This example could represent the Command Code "Edit Table Entry." The value 03 (Hex) would represent the File number in the high byte, and the 0A (Hex) would represent the remainder of the Command Code in the low byte.

Addressing High and Low Word of DWord Parameters

Double Word parameters are addressed in a similar fashion to the high and low bytes of a Word Parameter. For example, a DWord that begins in V2300 consumes both V2300 and V2301. The Low Word is V2300, and the High Word is V2301.



Input Function Status/Control Bits and Parameters

Input Function Status Bit Definitions

Input function offsets are listed in the order of Ch1/Fn1, Ch1/Fn2, Ch2/Fn1, Ch2/Fn2

Ch(x)/Fn(x) Status Bits (Transfers from CTRIO(2) to CPU)	Bit Offsets: WinPLC, EBC, PBC, DEVNETS, MODBUS	V-memory Offsets *Direct*LOGIC PLCs
Count Capture Complete Bit	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8
Timer Capture Start	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8
Timer Capture Complete (Timing) OR At Reset Value (Counting)	1, 9, 17, 25	20.1, 20.9, 21.1, 21.9
Timer "Timed Out" Bit	2, 10, 18, 26	20.2, 20.10, 21.2, 21.10
Pulse Catch Output Pulse State	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8
Pulse Catch Start	1, 9, 17, 25	20.1, 20.9, 21.1, 21.9

Input Function Control Bit Definitions

Input function offsets are listed in the order of Ch1/Fn1, Ch1/Fn2, Ch2/Fn1, Ch2/Fn2

Ch(n)/Fn(n) Control Bits (Transfers from CPU to CTRIO(2))	Bit Offsets: WinPLC, EBC, PBC, DEVNETS, MODBUS	V-memory Offsets *Direct*LOGIC PLCs
Enable Count Capture	0, 8, 16, 24	24.0, 24.8, 25.0, 25.8
Enable Timer Capture	0, 8, 16, 24	24.0, 24.8, 25.0, 25.8
Enable Pulse Catch	0, 8, 16, 24	24.0, 24.8, 25.0, 25.8
Reset	1, 9, 17, 25	24.1, 24.9, 25.1, 25.9

Input Function Status DWord Parameters

Input function offsets are listed in the order of Ch1/Fn1, Ch1/Fn2, Ch2/Fn1, Ch2/Fn2 and are in decimal format.

DWord Status CTRIO(2) to CPU	DWord Offsets: WinPLC, EBC, PBC, DEVNETS, MODBUS	V-memory Offsets from Output Start (octal)
DWord Parameter 1	0, 2, 4, 6	0, 4, 10, 14
DWord Parameter 2	1, 3, 5, 7	2, 6, 12, 16

Configured Function from CTRIO Workbench	Parameter 1 Contents DWORD	Parameter 2 Contents DWORD
Non-scaled Counter	Raw Input Value	Not Used
Scaled Counter	Scaled Value (pos. or rate)	Raw Value
Non-scaled Counter with Capture	Raw Value	Captured Value
Scaled Counter with Capture	Scaled Value (pos. or rate)	Captured Value
Non-scaled Timer	Previous Time (µs)	In Progress Time (µs)
Scaled Timer	Scaled Interval (rate)	In Progress Time (µs)
Pulse Catch	Not Used	Not Used

***NOTE**: If you select the 'discrete on chx/fnx' option for an input channel using pulse catch mode, you will get a message when you exit the I/O config screen noting 'pulse follower mode' or 'Pulse extension mode' for this output channel. This means only that the output will pulse for the specified duration when the input receives a sufficiently long pulse input.*

Example Input Control/Status Bits and Parameter Register Addresses

The following tables provide example addresses based on V2000 selected for the base input address and V2030 selected for the base output address. The Input Functions discussed on the following pages use these example addresses.

Status Registers: Example using V2000 as base input address for Input Channel 1 (Status bits and DWords received from CTRIO(2) to CPU)

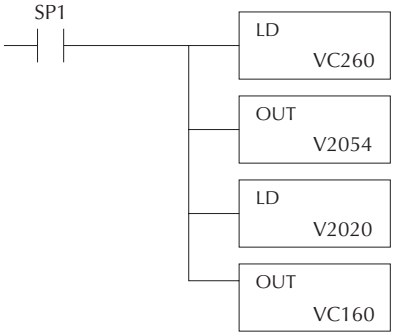
Name	PLC Example 1: Bit-of-Word (see note 2) DL05, DL06, D2-250-1/260, D4-450	PLC Example 2: Control Relay (see note 1) D2-240	Value
Counter Capture Complete Bit	V2020.0	C160	ON when Capture is completed
Timer Capture Starting	V2020.0	C160	On when Timer Capture begins
Timer Capture Complete (Timing) OR At Reset Value (Counting)	V2020.1	C161	ON when Timer Capture completes
Timer "Timed Out" Bit	V2020.2	C162	On when specified Timer "Time Out" period is exceeded
Pulse Catch Output Pulse State	V2020.0	C160	ON for the specified pulse time if input pulse qualifies as a valid pulse
Pulse Catch Starting	V2020.1	C161	ON when pulse edge occurs
Parameter 1	V2001–V2000	V2001–V2000	Decimal
Parameter 2	V2003–V2002	V2003–V2002	Decimal

Control Registers: Example using V2030 as base output address for Input Channel 1 (Control bits sent from CPU to CTRIO(2))

Name	PLC Example 1: Bit-of-Word (see note 2) DL05, DL06, D2-250-1/260, D4-450	PLC Example 2: Control Relay (see note 1), D2-240 CPU	Data Format
Enable Counter Capture	V2054.0	C260	Bit
Enable Timer Capture	V2054.0	C260	Bit
Enable Pulse Catch	V2054.0	C260	Bit
Reset	V2054.1	C261	Bit

Memory Mapping Example for D2-240 CPU

NOTE 1: *The D2-240 CPU does not support bit-of-word addressing. The status and control bits must be mapped to control relay words. An example of mapping code is shown below.*



NOTE 2: *For example,* ***Direct****SOFT uses B2020.1 in the ladder code to indicate that you are addressing the second bit of V-memory register V2020. The "B" prefix indicates bit-of-word addressing.*

Status Bits: Example using V2000 as base input address For Output Channel 1 (Status bits received from CTRIO(2) to CPU)

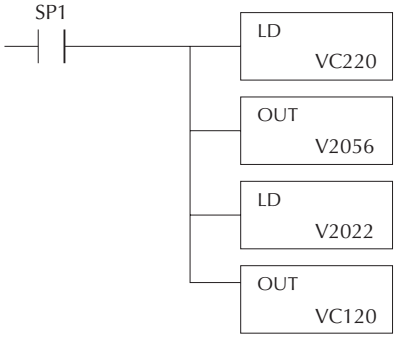
Name	PLC Example 1: Bit-of-Word (see note 2) DL05, DL06 D2-250-1/260, D4-450	PLC Example 2: Control Relay (see note 1) D2-240	Value
Output Enabled	V2022.0	C120	ON when Enable Output is ON
Position Loaded	V2022.1	C121	Used for Dynamic Positioning
Output Suspended	V2022.2	C122	ON when Output pulse is suspended
Output Active	V2022.4	C124	ON when Output is Pulsing
Output Stalled	V2022.5	C125	CTRIO Output Fault (should never be ON)
Command Error	V2022.6	C126	ON if Command or Parameters are invalid
Command Complete	V2022.7	C127	ON if Module receives Process Command

Control Bits/Registers: Example using V2030 as base output address for Output Channel 1 (Control DWords, Words, and bits sent from CPU to CTRIO(2))

Name	PLC Example 1: Bit-of-Word (see note 2), DL-05, DL06 D2-250-1/260, D4-450	PLC Example 2: Control Relay (see note 1), D2-240 CPU
Command Code	V2040	V2040
Parameter 1	V2041	V2041
Parameter 2	V2042	V2042
Parameter 3	V2031– V2030	V2031–V2030
Enable Output	V2056.0	C220
Go to Position	V2056.1	C221
Suspend Output	V2056.2	C222
Direction	V2056.4	C224
Process Command	V2056.7	C227

Memory Mapping Example for D2-240 CPU

NOTE 1: *The D2-240 CPU does not support bit-of-word addressing. The status and control bits must be mapped to control relay words. An example of mapping code is shown below.*



NOTE 2: *For example,* ***Direct****SOFT uses B2022.2 in the ladder code to indicate that you are addressing the third bit of V-memory register V2022. The "B" prefix indicates bit-of-word addressing.*