Input Functions

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Input Memory Mapping for Counter Data Transfer

☑ DL
☑ Win
☑ NI

The Counter function is used to create counts from an attached encoder. To use this function, one input needs to be configured as a Counter or Quad Counter.

The following table shows which memory locations are used for memory transfers from the CTRIO(2) module to the CPU. The starting memory location is defined by the user in the I/O Map within CTRIO Workbench. For the *Direct*LOGIC CPU, memory address offsets are in the second column. When using H2-WinPLC, EBC, PBC, MODBUS, or DEVNETS CPUs in the CPU slot, use the non-PLC offsets in column one.

The proper sequence of events for using this function can be found in the flow charts shown in later pages following.

Data Type and Offset WinPLC, EBC, PBC, DEVNETS, MODBUS	Address for Inputs (*Direct*LOGIC)	Definition	Format	Bytes
dwX0	n+0	Ch 1/Fn 1 Parameter 1	DWord	4
dwX1	n+2	Ch 1/Fn 1 Parameter 2		
dwX2	n+4	Ch 1/Fn 2 Parameter 1		
dwX3	n+6	Ch 1/Fn 2 Parameter 2		
dwX4	n+10	Ch 2/Fn 1 Parameter 1		
dwX5	n+12	Ch 2/Fn 1 Parameter 2		
dwX6	n+14	Ch 2/Fn 2 Parameter 1		
dwX7	n+16	Ch 2/Fn 2 Parameter 2		
bX0...7 bX8...15	n+20	Ch 1/Fn 1 Status (Low Byte) Ch 1/Fn 2 Status (High Byte)	Word	2
bX16...23 bX24...31	n+21	Ch 2/Fn 1 Status (Low Byte) Ch 2/Fn 2 Status (High Byte)		
bX32...39 bX40...47	n+22	Output 0 Status (Low Byte) Output 1 Status (High Byte)		
bX48...55 bX56...63	n+23	Output 2 Status (Low Byte) Output 3 Status (High Byte)		
bX64...71 bX72...79 bX80...87 bX88...95	n+24	System Functions Read/Write CTRIO(2) Internal Registers (see p. 6-10 for bit definitions)	DWord	4
				44 Total Bytes

Example Input Control/Status Bits and Parameter Register Addresses

The following tables provide example addresses based on V2000 selected for the base input address. The Input Functions discussed on the following pages use these example addresses.

Input(n) Parameter Definitions

Parameter values are in Decimal format.

Configured Function from CTRIO Workbench	Parameter 1 Contents DWORD	Parameter 2 Contents DWORD
Non-scaled Counter	Raw Input Value	Not Used
Scaled Counter	Scaled Value (pos. or rate)	Raw Value
Non-scaled Counter with Capture	Raw Value	Captured Value
Scaled Counter with Capture	Scaled Value (pos. or rate)	Scaled Captured Value
Non-scaled Timer	Previous Time (µs)	In Progress Time (µs)
Scaled Timer	Scaled Interval (rate)	Scaled In Progress Time (µs)
Pulse Catch	Not Used	Not Used

Counter & Quadrature Counter

Parameter 1 and 2 values, shown in the table above, will be mapped to V2000 - V2003 in this example. If input D is configured for Count Capture, the Enable Count Capture bit (see table below) must be ON in order for input D to be able to snapshot the current count. The Counter Capture Complete bit is used to indicate the acquisition has occurred. The program will need to turn OFF the Enable Capture and confirm the Capture Complete bit resets before attempting the next count capture. The Reset bit will reset raw and scaled values to the specified reset value. The last captured value, if applicable, will remain at V2054.

Name	PLC Control Outputs Base Addr = V2030 (Bit-of-Word)	PLC Status Inputs Base Addr = V2000 (Bit-of-Word)	PLC Control Outputs Base Addr = V2030 (Control Relay) D2-240	PLC Status Inputs Base Addr = V2000 (Control Relay) D2-240	Description
Parameter 1	N/A	V2001-V2000	N/A	V2001-V2000	Refer to table above
Parameter 2		V2003-V2002		V2003-V2002	Refer to table above
Counter Capture Complete		V2020.0		C160	On when Count Capture is completed (Available only when input D is configured for Capture input)
Enable Count Capture	V2054.0	N/A	C260	N/A	Turn ON to capture Count (Available only when input D is configured for Capture input)
Reset	V2054.1		C261		Turn ON to reset Counter Value to Reset Value
At Reset Value	N/A	V2020.1	N/A	C161	On when Counter is at Reset Value

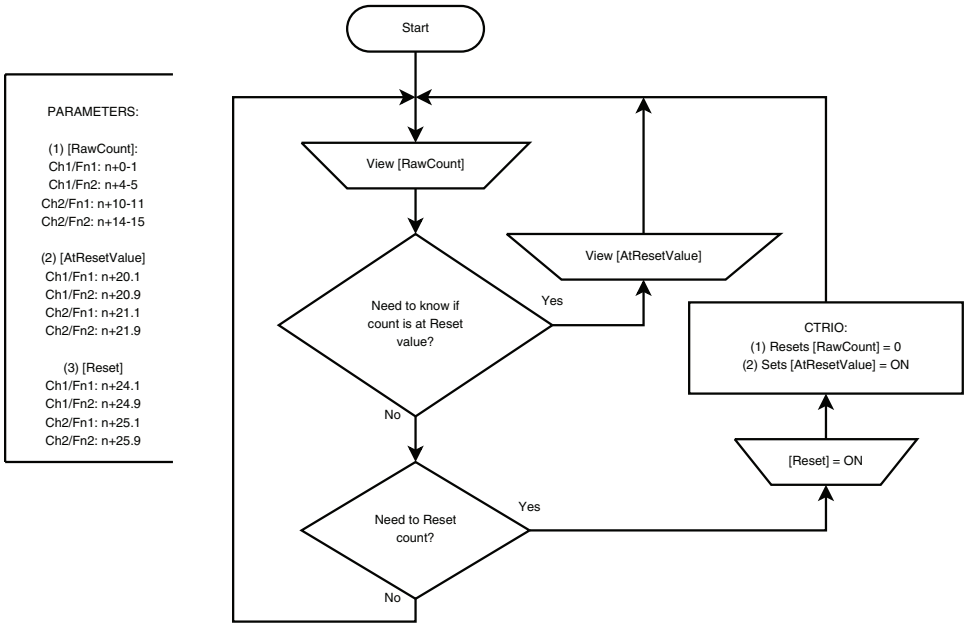
NOTE: For DirectSOFT users: the I/O Map dialog displays the exact memory locations in use by the CTRIO(2) module. Within the I/O Map dialog you can print out a report of memory locations in use.

Input Function Status Bit Definitions

Input function offsets are listed in the order of Ch1/Fn1, Ch1/Fn2, Ch2/Fn1, Ch2/Fn2

Ch(x)/Fn(x) Status Bits (transfers from CTRIO(2) to CPU)	Bit Offsets: WinPLC, EBC, PBC, DEVNETS, MODBUS	V-memory Offsets DirectLOGIC PLCs
Count Capture Complete Bit	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8

Counter Function (IBoxes & DL-PLC

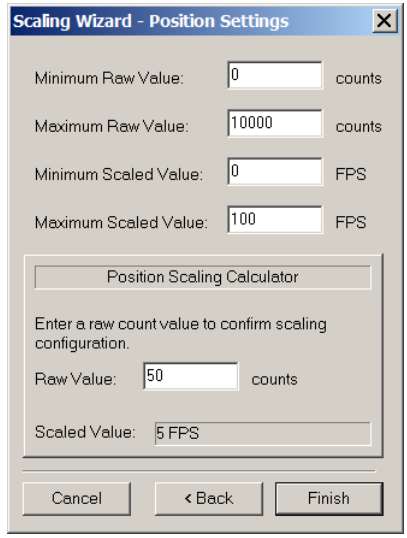


Input Memory Map for Scaled Counter Data

☑ DL
☑ Win
☑ NI

Scaled Counter is simply used to create counts in user-specified engineering units from an attached encoder. To use this function, one input needs to be configured as a Counter or Quad Counter. Then, for that Input functions, select the ruler icon and use the wizard to configure the desired engineering units.

This is the final panel in the Scaling Wizard. Be sure to use the Position Scaling Calculator to validate that the Raw Value (raw counts from the encoder) will generate the desired Scaled Value. Type in the test counts (50 is shown here) and verify the expected engineering units value is displayed in the Scaled Value field. It will be displayed with the Engineering Units characters provided earlier in the Wizard. FPS (feet per second) was used here. The Calculator returned '5FPS' here.



The following table shows which memory locations are used for memory transfers from the CTRIO(2) module to the CPU. The starting memory location is defined by the user in the I/O Map within CTRIO Workbench. When configuring the *Direct*LOGIC CPU, use the memory address offsets in the second column. When configuring an H2-WinPLC, EBC, PBC, MODBUS, or DEVNETS placed in the CPU slot, use the non-PLC offsets in column one.

Data Type and Offset WinPLC, EBC, PBC, DEVNETS, MODBUS	Address for Inputs (*Direct*LOGIC)	Definition	Format	Bytes
dwX0	n+0	Ch 1/Fn 1 Parameter 1	DWord	4
dwX1	n+2	Ch 1/Fn 1 Parameter 2		
dwX2	n+4	Ch 1/Fn 2 Parameter 1		
dwX3	n+6	Ch 1/Fn 2 Parameter 2		
dwX4	n+10	Ch 2/Fn 1 Parameter 1		
dwX5	n+12	Ch 2/Fn 1 Parameter 2		
dwX6	n+14	Ch 2/Fn 2 Parameter 1		
dwX7	n+16	Ch 2/Fn 2 Parameter 2		
bX0...7 bX8...15	n+20	Ch 1/Fn 1 Status (Low Byte) Ch 1/Fn 2 Status (High Byte)	Word	2
bX16...23 bX24...31	n+21	Ch 2/Fn 1 Status (Low Byte) Ch 2/Fn 2 Status (High Byte)		
bX32...39 bX40...47	n+22	Output 0 Status (Low Byte) Output 1 Status (High Byte)		
bX48...55 bX56...63	n+23	Output 2 Status (Low Byte) Output 3 Status (High Byte)		
bX64...71 bX72...79 bX80...87 bX88...95	n+24	System Functions Read/Write CTRIO(2) Internal Registers (see p. 6-10 for bit definitions)	DWord	4
				44 Total Bytes

Input(n) Parameter Definitions

Parameter values are in Decimal format.

Configured Function from CTRIO Workbench	Parameter 1 Contents DWORD	Parameter 2 Contents DWORD
Non-scaled Counter	Raw Input Value	Not Used
Scaled Counter	Scaled Value (pos. or rate)	Raw Value
Non-scaled Counter with Capture	Raw Value	Captured Value
Scaled Counter with Capture	Scaled Value (pos. or rate)	Scaled Captured Value
Non-scaled Timer	Previous Time (µs)	In Progress Time (µs)
Scaled Timer	Scaled Interval (rate)	Scaled In Progress Time (µs)
Pulse Catch	Not Used	Not Used

Counter & Quadrature Counter

Parameters 1 and 2 are explained above and will be mapped to V2000 - V2003 in this example. If input D is configured for Count Capture, the Enable Count Capture bit must be ON in order for input D to be able to snapshot the current count. The Counter Capture Complete bit is used to indicate the acquisition has occurred. The program will need to turn OFF the Enable Capture and confirm the Capture Complete bit resets before attempting the next count capture. The Reset bit will reset raw and scaled values to the specified reset value. The last captured value, if applicable, will remain.

Name	PLC Control Outputs Base Addr = V2030 (Bit-of-Word)	PLC Status Inputs Base Addr = V2000 (Bit-of-Word)	PLC Control Outputs Base Addr = V2030 (Control Relay) D2-240	PLC Status Inputs Base Addr = V2000 (Control Relay) D2-240	Description
Parameter 1	N/A	V2001-V2000	N/A	V2001-V2000	Refer to table above
Parameter 2		V2003-V2002		V2003-V2002	Refer to table above
Counter Capture Complete		V2020.0		C160	On when Count Capture is completed (Available only when input D is configured for Capture input)
Enable Count Capture	V2054.0	N/A	C260	N/A	Turn ON to capture Count (Available only when input D is configured for Capture input)
Reset	V2054.1		C261		Turn ON to reset Counter Value to Reset Value
At Reset Value	N/A	V2020.1	N/A	C161	On when Counter is at Reset Value

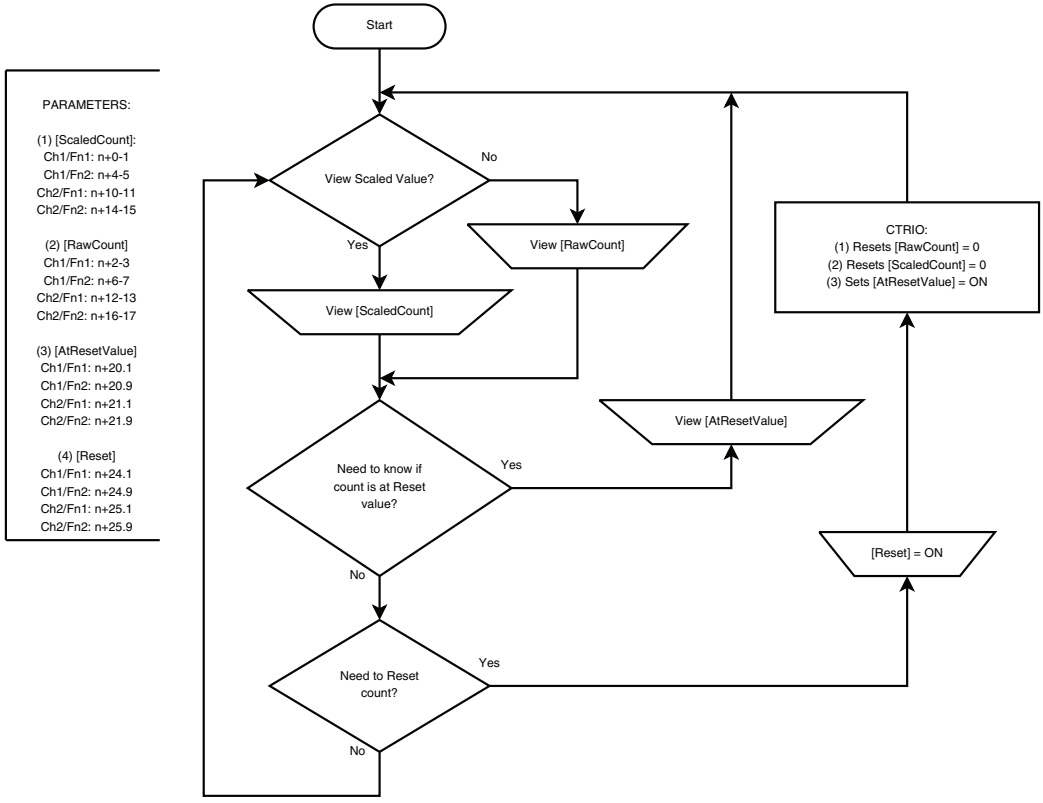
NOTE: *For* ***Direct****SOFT users: the* ***I/O Map*** *dialog displays the exact memory locations in use by the CTRIO(2) module. Within the I/O Map dialog you can print out a report of memory locations in use.*

Input Function Status Bit Definitions

Input function offsets are listed in the order of Ch1/Fn1, Ch1/Fn2, Ch2/Fn1, Ch2/Fn2

Ch(x)/Fn(x) Status Bits (Transfers from CTRIO(2) to CPU)	Bit Offsets: WinPLC, EBC, PBC, DEVNETS, MODBUS	V-memory Offsets *Direct*LOGIC PLCs
Count Capture Complete Bit	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8

Counter Function (Scaled) (IBoxes & DL-PLC)



Input Memory Map for Capture Count Data Transfers

☑ DL
☑ Win
☑ NI

This function copies the current value of a counter input into a register when a discrete input trigger condition is met. To use this function, one input must be configured as a Counter or Quad Counter and one as Capture Fn. An input must be set as a counter before Capture Fn will appear in the menu of CTRIO Workbench dialog box.

The following table shows which memory locations are used for memory transfers from the CTRIO(2) module to the CPU. The starting memory location is defined by the user in the I/O Map within CTRIO Workbench. When configuring the *Direct*LOGIC CPU, use the memory address offsets in the second column. When configuring an H2-WinPLC, EBC, PBC, MODBUS, or DEVNETS placed in the CPU slot, use the non-PLC offsets in column one.

The proper sequence of events for using this function can be found in the flow charts on the pages that follow.

Data Type and Offset WinPLC, EBC, PBC, DEVNETS, MODBUS	Address for Inputs (*Direct*LOGIC)	Definition	Format	Bytes
dwX0	n+0	Ch 1/Fn 1 Parameter 1	DWord	4
dwX1	n+2	Ch 1/Fn 1 Parameter 2		
dwX2	n+4	Ch 1/Fn 2 Parameter 1		
dwX3	n+6	Ch 1/Fn 2 Parameter 2		
dwX4	n+10	Ch 2/Fn 1 Parameter 1		
dwX5	n+12	Ch 2/Fn 1 Parameter 2		
dwX6	n+14	Ch 2/Fn 2 Parameter 1		
dwX7	n+16	Ch 2/Fn 2 Parameter 2		
bX0...7 bX8...15	n+20	Ch 1/Fn 1 Status (Low Byte) Ch 1/Fn 2 Status (High Byte)	Word	2
bX16...23 bX24...31	n+21	Ch 2/Fn 1 Status (Low Byte) Ch 2/Fn 2 Status (High Byte)		
bX32...39 bX40...47	n+22	Output 0 Status (Low Byte) Output 1 Status (High Byte)		
bX48...55 bX56...63	n+23	Output 2 Status (Low Byte) Output 3 Status (High Byte)		
bX64...71 bX72...79 bX80...87 bX88...95	n+24	System Functions Read/Write CTRIO(2) Internal Registers (see p. 6-10 for bit definitions)	DWord	4
				44 Total Bytes

Input(n) Parameter Definitions

Parameter values are in Decimal format.

Configured Function from CTRIO Workbench	Parameter 1 Contents DWORD	Parameter 2 Contents DWORD
Non-scaled Counter	Raw Input Value	Not Used
Scaled Counter	Scaled Value (pos. or rate)	Raw Value
Non-scaled Counter with Capture	Raw Value	Captured Value
Scaled Counter with Capture	Scaled Value (pos. or rate)	Scaled Captured Value
Non-scaled Timer	Previous Time (μs)	In Progress Time (μs)
Scaled Timer	Scaled Interval (rate)	Scaled In Progress Time (μs)
Pulse Catch	Not Used	Not Used

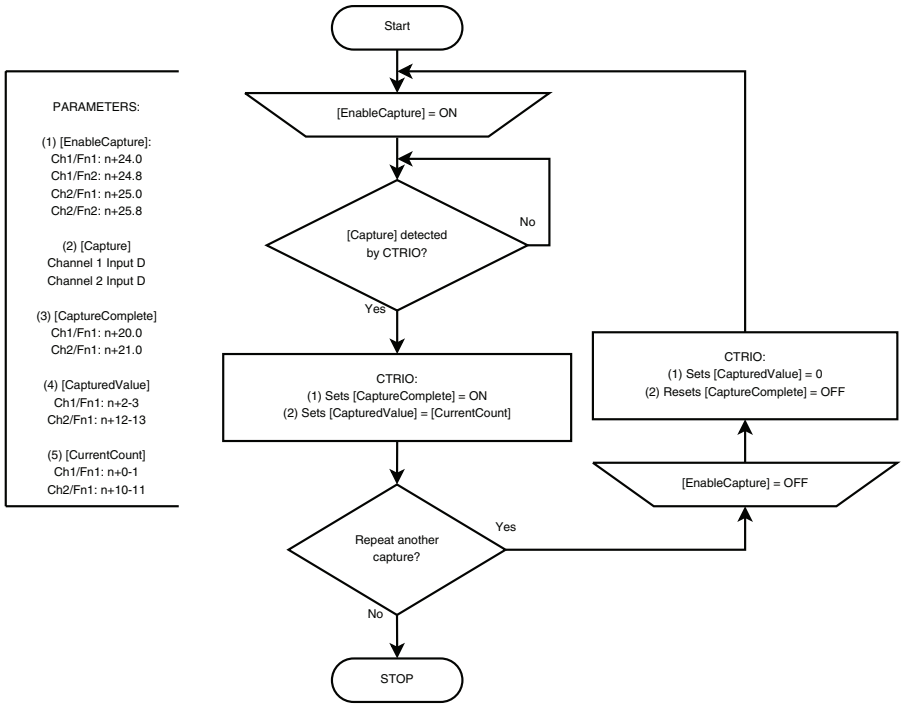
NOTE: *For* ***Direct****SOFT users: the* ***I/O Map*** *dialog displays the exact memory locations in use by the CTRIO(2) module. Within the I/O Map dialog you can print out a report of memory locations in use.*

Input Function Status Bit Definitions

Input function offsets are listed in the order of Ch1/Fn1, Ch1/Fn2, Ch2/Fn1, Ch2/Fn2

Ch(x)/Fn(x) Status Bits (Transfers from CTRIO(2) to CPU)	Bit Offsets: WinPLC, EBC, PBC, DEVNETS, MODBUS	V-memory Offsets *Direct*LOGIC PLCs
Count Capture Complete Bit	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8
Timer Capture Start	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8
Timer Capture Complete (Timing) OR At Reset Value (Counting)	1, 9, 17, 25	20.1, 20.9, 21.1, 21.9
Timer "Timed Out" Bit	2, 10, 18, 26	20.2, 20.10, 21.2, 21.10
Pulse Catch Output Pulse State	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8
Pulse Catch Start	1, 9, 17, 25	20.1, 20.9, 21.1, 21.9

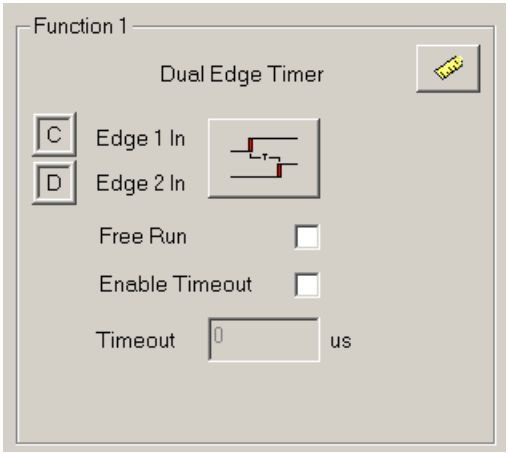
Capture Count Function (IBoxes & DL-PLC)



Input Memory Map for Edge Timer and Dual Edge Timer

☑ DL
☑ Win
☑ NI

Edge Timer and Dual Edge Timer are used to precisely measure the time between two discrete input events. To use one of these functions, configure one input as Edge Timer or configure two inputs as Dual Edge Timer. Then cycle through the various edge options by repeatedly pressing the button with the graphic depiction of the signal edges.



Function one shows the configuration for a Dual Edge Timer that will time from the rising edge of Input C to the rising edge of Input D. Free Run is not selected and Enable Timeout is not selected. There is no scaling. If Scaling were selected, the time result would be in the selected engineering units.

Running an Edge Timer with the default settings takes the least supporting code to operate. The default settings are Free Run disabled and Enable Timeout disabled.

When Free Run is enabled, the timer will start as soon as Edge 1 In is true. With Free Run enabled, the timer will always show the last valid capture value; or, 0 if the last measurement resulted in a timeout.

When Free Run is disabled, the timer will start when Enable Capture and Edge 1 are true. With Free Run disabled, the timer will show the last time captured.

When Enable Timeout is enabled, the timer will timeout if the Edge 2 event does not occur before the timeout timer expires. The timeout timer starts when Enable Capture is true and Edge 1 becomes true. When a timeout occurs, the Timeout and Capture Complete bit are set and the Timer and Last Time values are cleared.

When Enable Timeout is disabled, once Edge 1 event is true, the timer will run until Edge 2 event becomes true.

The behavior resulting from various combinations of the options above can also be found in the flow charts that follow.

The following table shows which memory locations are used for memory transfers from the CTRIO(2) module to the CPU. The starting memory location is defined by the user in the I/O Map within CTRIO Workbench. When configuring the *Direct*LOGIC CPU, use the memory address offsets in the second column. When configuring an H2-WinPLC, EBC, PBC, MODBUS, or DEVNETS placed in the CPU slot, use the non-PLC offsets in column one.

Data Type and Offset WinPLC, EBC, PBC, DEVNETS, MODBUS	Address for Inputs (*Direct*LOGIC)	Definition	Format	Bytes
dwX0	n+0	Ch 1/Fn 1 Parameter 1	DWord	4
dwX1	n+2	Ch 1/Fn 1 Parameter 2		
dwX2	n+4	Ch 1/Fn 2 Parameter 1		
dwX3	n+6	Ch 1/Fn 2 Parameter 2		
dwX4	n+10	Ch 2/Fn 1 Parameter 1		
dwX5	n+12	Ch 2/Fn 1 Parameter 2		
dwX6	n+14	Ch 2/Fn 2 Parameter 1		
dwX7	n+16	Ch 2/Fn 2 Parameter 2		
bX0...7 bX8...15	n+20	Ch 1/Fn 1 Status (Low Byte) Ch 1/Fn 2 Status (High Byte)	Word	2
bX16...23 bX24...31	n+21	Ch 2/Fn 1 Status (Low Byte) Ch 2/Fn 2 Status (High Byte)		
bX32...39 bX40...47	n+22	Output 0 Status (Low Byte) Output 1 Status (High Byte)		
bX48...55 bX56...63	n+23	Output 2 Status (Low Byte) Output 3 Status (High Byte)		
bX64...71 bX72...79 bX80...87 bX88...95	n+24	System Functions Read/Write CTRIO(2) Internal Registers (see p. 6-10 for bit definitions)	DWord	4
				44 Total Bytes

Input(n) Parameter Definitions

Parameter values are in Decimal format.

Configured Function from CTRIO Workbench	Parameter 1 Contents DWORD	Parameter 2 Contents DWORD
Scaled Counter with Capture	Scaled Value (pos. or rate)	Scaled Captured Value
Non-scaled Timer	Previous Time (µs)	In Progress Time (µs)
Scaled Timer	Scaled Interval (rate)	Scaled In Progress Time (µs)

Input(n) Parameter Edge Timer and Dual Edge Timer

Parameters 1 and 2 are explained and will be mapped to V2000 - V2003 in this example.

Standard Timers:

When the Enable Timer Capture bit is ON and the configured input edge occurs, the CTRIO(2) module will begin timing. The Timer Capture Starting bit will be ON while the timing is in progress and will turn OFF when the next configured input edge occurs and the Timer Capture Complete bit turns ON. The program will need to turn off the Enable Timer Capture bit, and confirm the Timer Capture Starting and Timer Capture Complete bits reset before attempting the next time capture cycle. Turning OFF the Enable Timer Capture bit resets the timers register values to zero.

Free Run Timers:

If the Free Run Timer option was configured, the Enable Timer Capture bit is not available. When the configured input edge occurs, the CTRIO(2) module will begin timing. The Timer Capture Starting bit will be ON while the timing is in progress and will turn OFF when the next configured input edge occurs. When this edge occurs, the Timer "in progress time" register resets to zero. The "previous time" register will always retain the most recent captured time value.

Name	PLC Control Outputs Base Addr = V2030 (Bit-of-Word)	PLC Status Inputs Base Addr = V2000 (Bit-of-Word)	PLC Control Outputs Base Addr = V2030 (Control Relay) D2-240	PLCStatus Inputs Base Addr = V2000 (Control Relay) D2-240	Description
Parameter 1	N/A	V2001-V2000	N/A	V2001-V2000	Previous Time
Parameter 2		V2003-V2002		V2003-V2002	In Progress Time
Timer Capture Starting		V2020.0		C160	On when Time Capture is in progress
Enable Timer Capture	V2054.0	N/A	C260	N/A	Turn ON to enable Timer Capture Function (Not available when Free Run Timer option is selected)
Timer Capture Complete	N/A	V2020.1	N/A	C161	On when Timing is completed
Timer Timeout Bit		V2020.2		C162	Set when Timeout Occurs

Edge and Dual Edge Timer Timeout Function

The Timer Timeout Function is available for use with standard and Free Run Timers. It is primarily used in Free Run timing of recurring events (rate, velocity calculations, etc.). The specified Timeout Period is in effect once the timer is enabled until receiving the first configured input edge. Then it is in effect until receiving the next edge of the timing input to complete the timing cycle.

Standard Timers:

Once the timer is enabled, the Timeout Bit is set if the time that it takes the CTRIO(2) module to see the configured input edge exceeds the specified Timeout Period. The program will need to turn off the Enable Timer Capture bit, and confirm the Timer Capture Complete bit and Timeout bit resets before attempting the next time capture cycle.

Once timing has been initiated, if the time before the CTRIO(2) module sees the next configured edge exceeds the specified Timeout Period, the Timeout bit is set. The Timer register values are reset to zero. The program will need to turn off the Enable Timer Capture bit, and confirm the Timer Capture Starting bit, Timer Capture Complete bit and the Timeout bit reset before attempting the next time capture cycle.

Free Run Timers:

The Timeout Bit is set if the time that it takes the CTRIO(2) module to see the configured input edge exceeds the specified Timeout Period. The Timeout bit resets when the next timing cycle begins. The "Previous Time" register value is reset to zero.

Once timing has been initiated, if the time before the CTRIO(2) module sees the next configured edge exceeds the specified Timeout Period, the Timeout bit is set. The Timer register values are reset to zero. The Timeout bit resets when the next timing cycle begins.

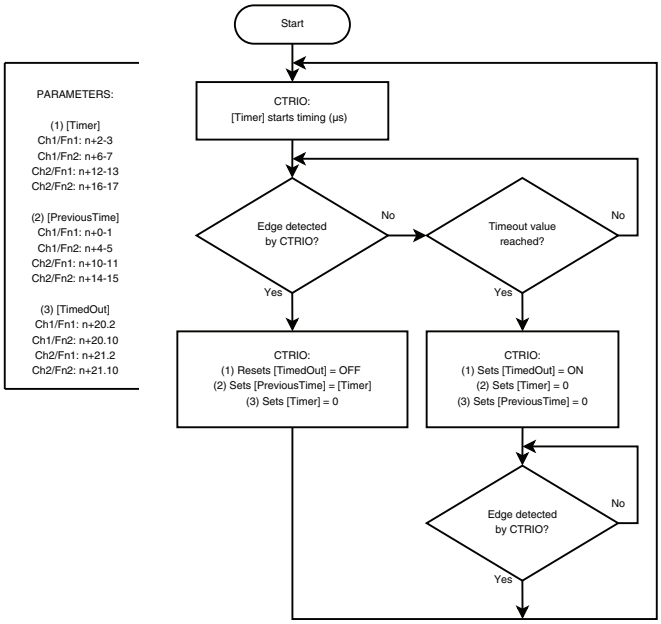
***NOTE:** For **Direct**SOFT users: the **I/O Map** dialog displays the exact memory locations in use by the CTRIO(2) module. Within the I/O Map dialog you can print out a report of memory loctions in use.*

Input Function Status Bit Definitions

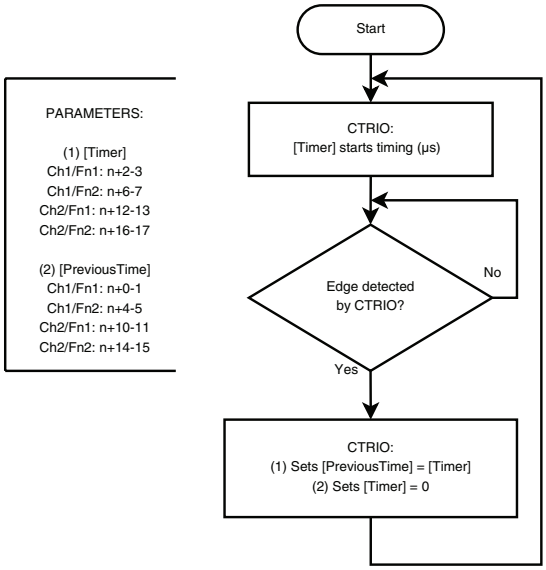
Input function offsets are listed in the order of Ch1/Fn1, Ch1/Fn2, Ch2/Fn1, Ch2/Fn2

Ch(x)/Fn(x) Status Bits (Transfers from CTRIO(2) to CPU)	Bit Offsets: WinPLC, EBC, PBC, DEVNETS, MODBUS	V-memory Offsets *Direct*LOGIC PLCs
Count Capture Complete Bit	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8
Timer Capture Start	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8
Timer Capture Complete (Timing) OR At Reset Value (Counting)	1, 9, 17, 25	20.1, 20.9, 21.1, 21.9
Timer "Timed Out" Bit	2, 10, 18, 26	20.2, 20.10, 21.2, 21.10
Pulse Catch Output Pulse State	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8
Pulse Catch Start	1, 9, 17, 25	20.1, 20.9, 21.1, 21.9

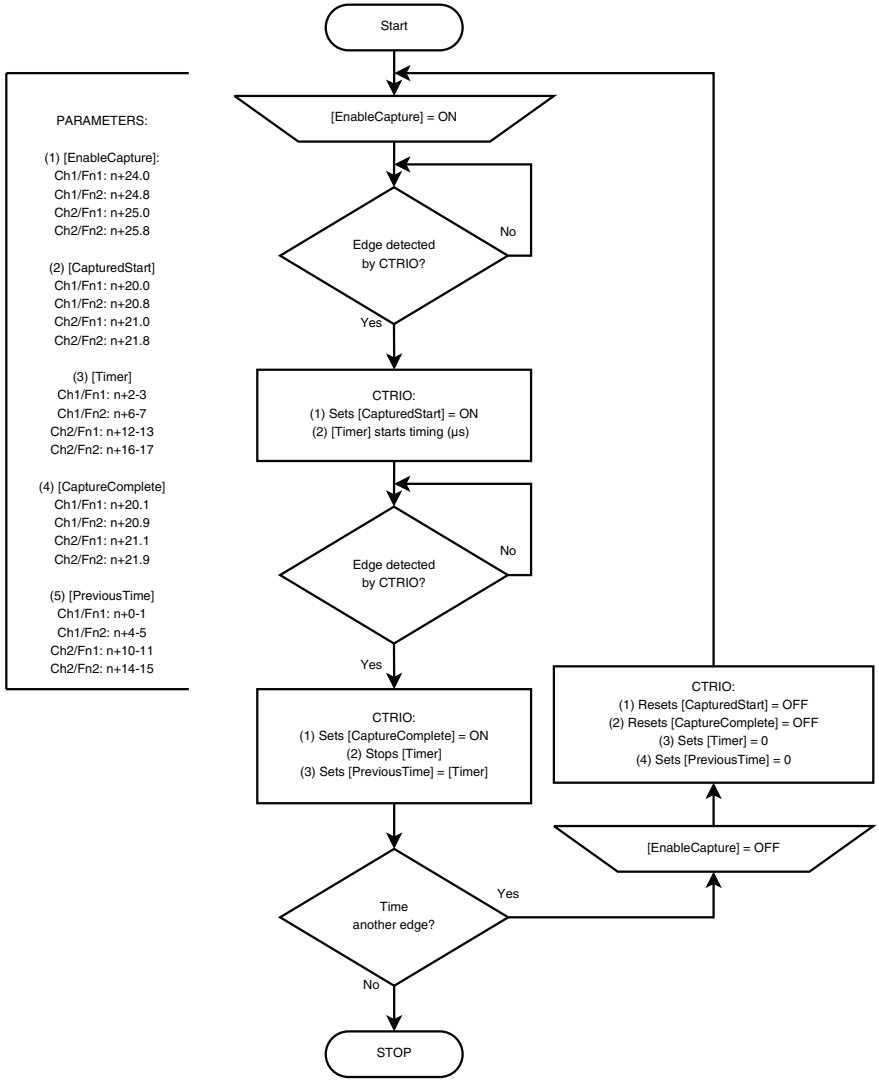
Edge Timer Function
(Free Run, Timeout)
(IBoxes)



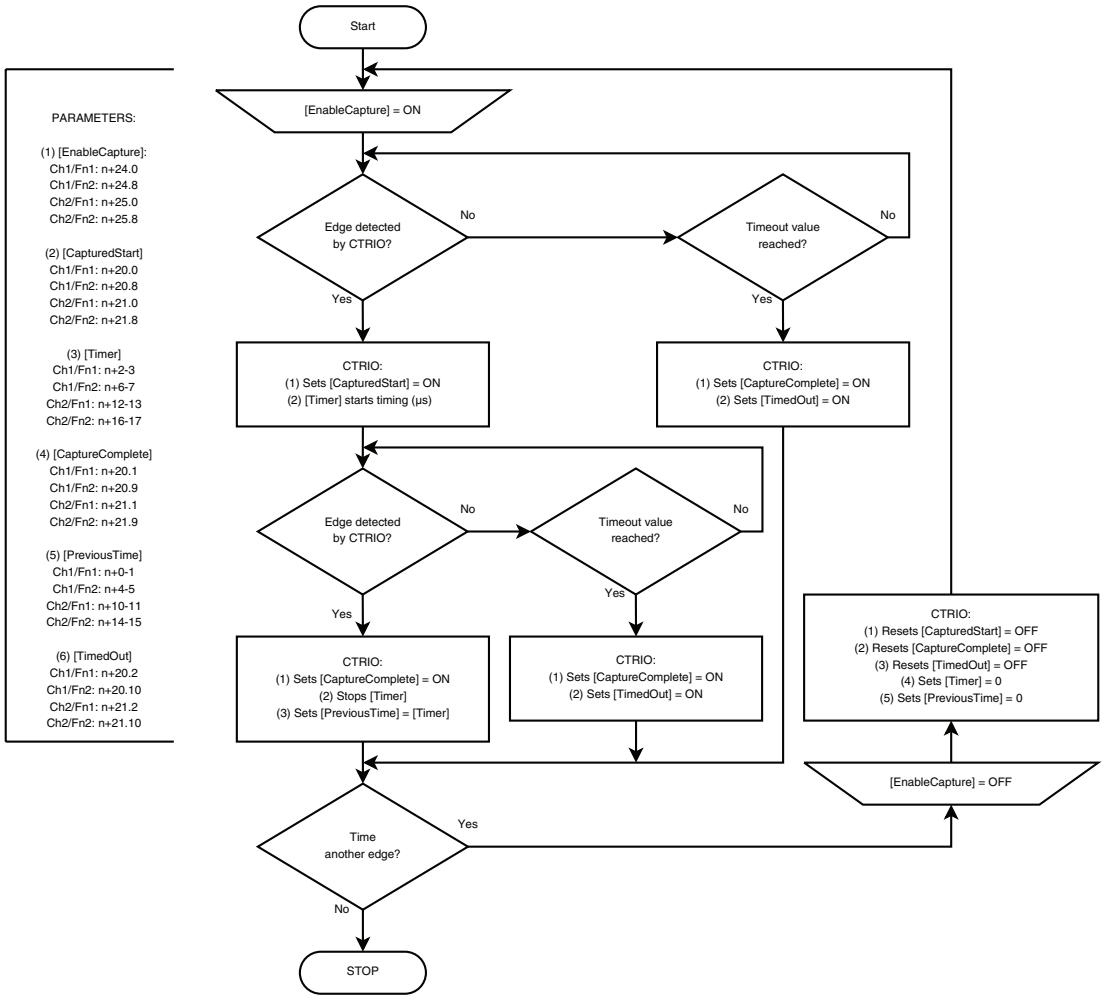
Edge Timer Function
(Free Run, No Timeout)
(IBoxes)



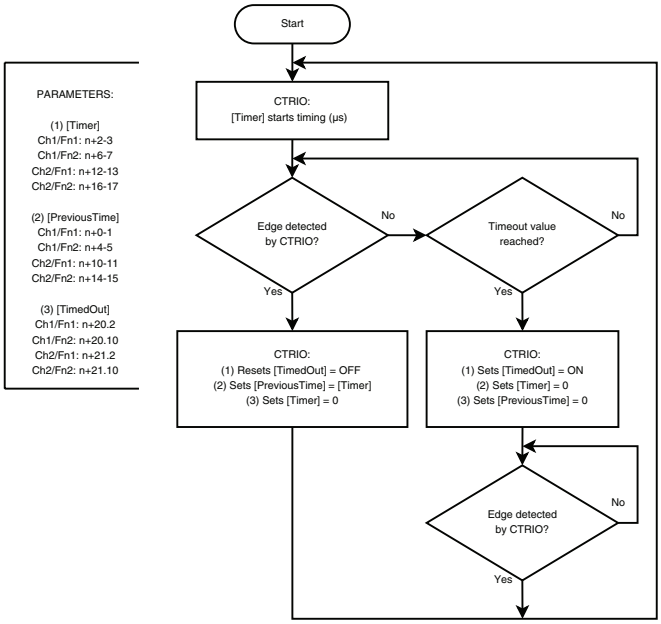
Edge Timer Function (Manual, No Timeout) (IBoxes)



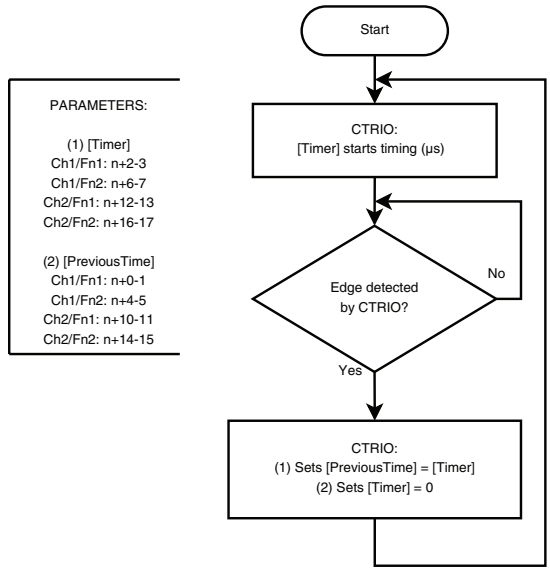
Edge Timer Function
(Manual, Timeout)
(IBoxes)



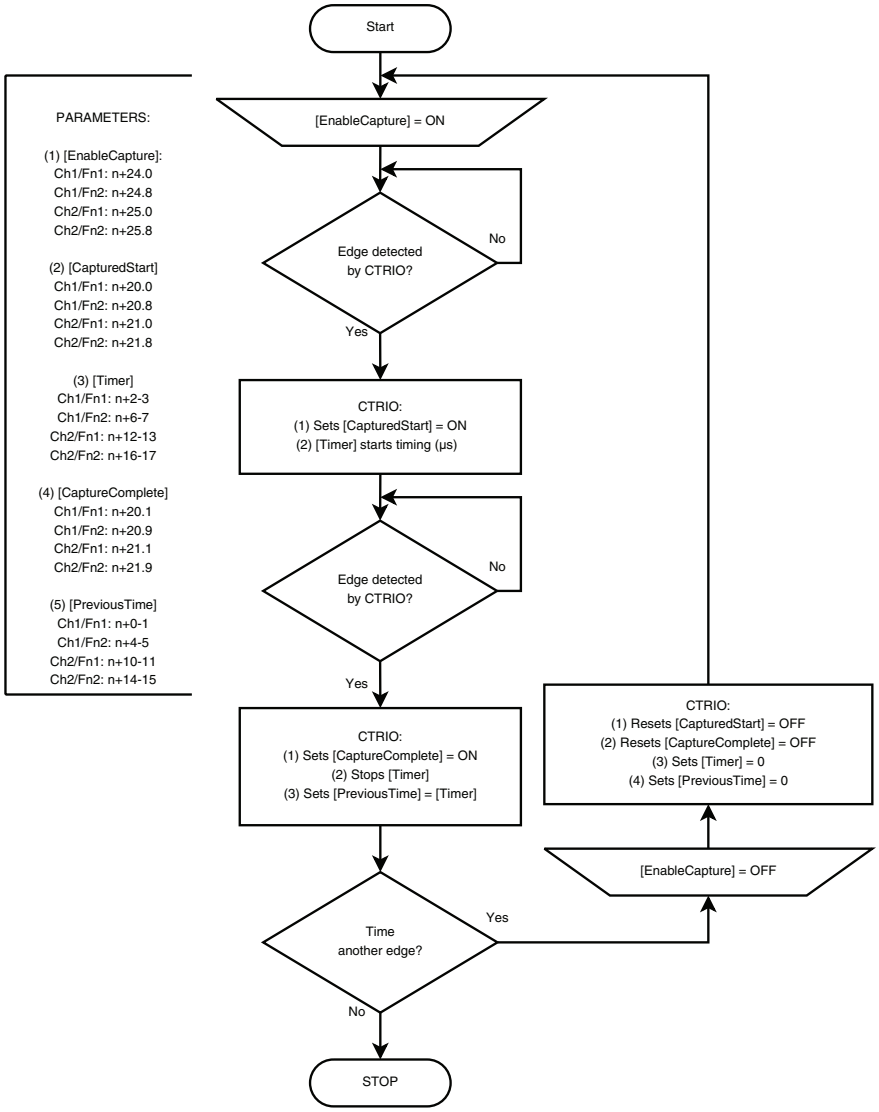
Edge Timer Function
(Free Run, Timeout)
(DL-PLC)



Edge Timer Function
(Free Run, No Timeout)
(DL-PLC)



Edge Timer Function (Manual, No Timeout) (DL-PLC)



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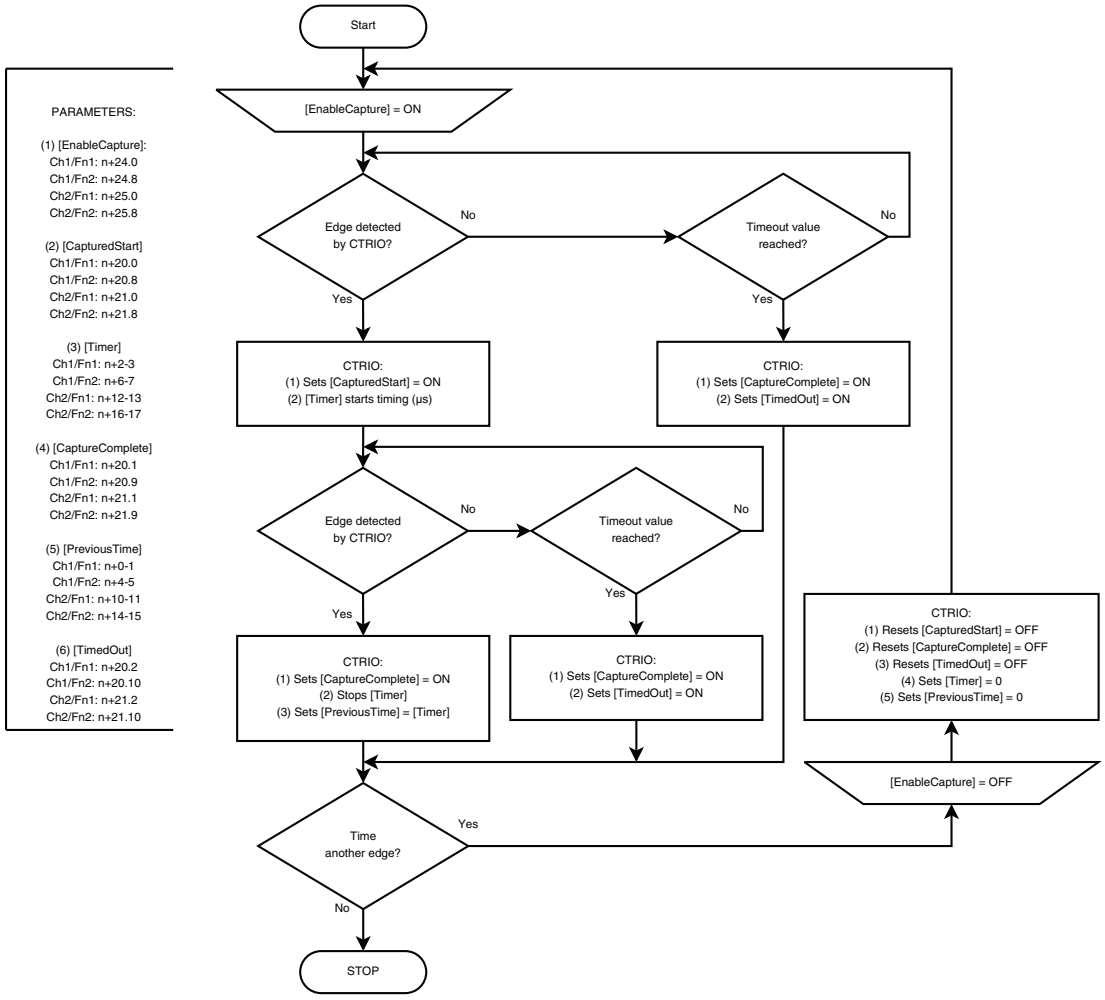


Inhibit

☑ DL
☑ Win
☑ NI

Inhibit allows an input of the CTRIO(2) to pause the counting of Function 1, a Quad Counter or simple Counter. To use this function, Input A must be configured as a Counter or Quad Counter. An input must be set as a counter before Inhibit Fn 1 will appear in the menu in CTRIO Workbench.

The following table shows which memory locations are used for memory transfers from the CTRIO(2) module to the CPU. The starting memory location is defined by the user in the I/O Map within CTRIO Workbench. When configuring the ***Direct***LOGIC CPU, use the memory address offsets in the second column. When configuring an H2-WinPLC, EBC, PBC, MODBUS, or DEVNETS placed in the CPU slot, use the non-PLC offsets in column one.

Data Type and Offset WinPLC, EBC, PBC, DEVNETS, MODBUS	Address for Inputs (*Direct*LOGIC)	Definition	Format	Bytes
dwX0	n+0	Ch 1/Fn 1 Parameter 1	DWord	4
dwX1	n+2	Ch 1/Fn 1 Parameter 2		
dwX2	n+4	Ch 1/Fn 2 Parameter 1		
dwX3	n+6	Ch 1/Fn 2 Parameter 2		
dwX4	n+10	Ch 2/Fn 1 Parameter 1		
dwX5	n+12	Ch 2/Fn 1 Parameter 2		
dwX6	n+14	Ch 2/Fn 2 Parameter 1		
dwX7	n+16	Ch 2/Fn 2 Parameter 2		
bX0...7 bX8...15	n+20	Ch 1/Fn 1 Status (Low Byte) Ch 1/Fn 2 Status (High Byte)	Word	2
bX16...23 bX24...31	n+21	Ch 2/Fn 1 Status (Low Byte) Ch 2/Fn 2 Status (High Byte)		
bX32...39 bX40...47	n+22	Output 0 Status (Low Byte) Output 1 Status (High Byte)		
bX48...55 bX56...63	n+23	Output 2 Status (Low Byte) Output 3 Status (High Byte)		
bX64...71 bX72...79 bX80...87 bX88...95	n+24	System Functions Read/Write CTRIO(2) Internal Registers (see p. 6-10 for bit definitions)	DWord	4
				44 Total Bytes

Input (n) Parameter Definitions

Parameter values are in Decimal format.

Configured Function from CTRIO Workbench	Parameter 1 Contents DWORD	Parameter 2 Contents DWORD
Non-scaled Counter	Raw Input Value	Not Used
Scaled Counter	Scaled Value (pos. or rate)	Raw Value
Non-scaled Counter with Capture	Raw Value	Captured Value
Scaled Counter with Capture	Scaled Value (pos. or rate)	Scaled Captured Value
Non-scaled Timer	Previous Time (µs)	In Progress Time (µs)
Scaled Timer	Scaled Interval (rate)	Scaled In Progress Time (µs)
Pulse Catch	Not Used	Not Used

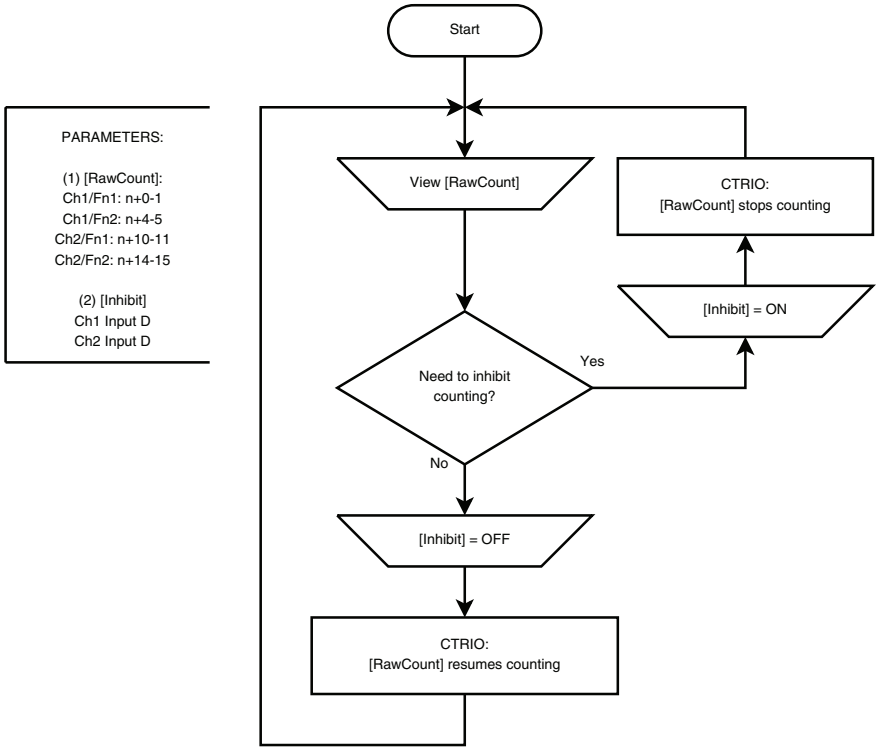
NOTE: *For* ***Direct****SOFT users: the* ***I/O Map*** *dialog displays the exact memory locations in use by the CTRIO(2) module. Within the I/O Map dialog you can print out a report of memory locations in use.*

Input Function Status Bit Definitions

Input function offsets are listed in the order of Ch1/Fn1, Ch1/Fn2, Ch2/Fn1, Ch2/Fn2

Ch(x)/Fn(x) Status Bits (Transfers from CTRIO(2) to CPU)	Bit Offsets: WinPLC, EBC, PBC, DEVNETS, MODBUS	V-memory Offsets *Direct*LOGIC PLCs
Count Capture Complete Bit	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8
Timer Capture Start	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8
Timer Capture Complete (Timing) OR At Reset Value (Counting)	1, 9, 17, 25	20.1, 20.9, 21.1, 21.9
Timer "Timed Out" Bit	2, 10, 18, 26	20.2, 20.10, 21.2, 21.10
Pulse Catch Output Pulse State	0, 8, 16, 24	20.0, 20.8, 21.0, 21.8
Pulse Catch Start	1, 9, 17, 25	20.1, 20.9, 21.1, 21.9

Inhibit Function (IBoxes & DL-PLC

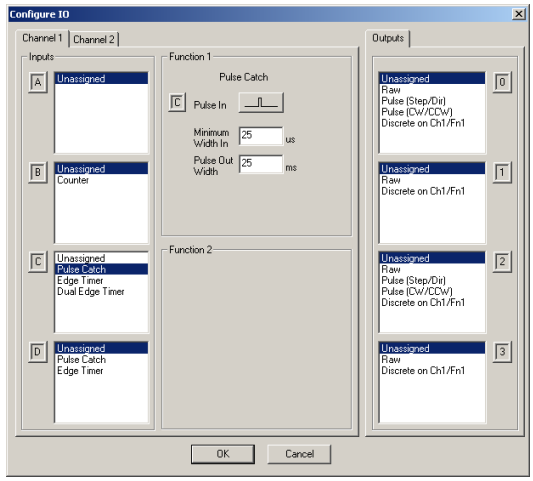


put Memory Map for Pulse Catch Data Transfers

☑ DL
☑ Win
☑ NI

The Pulse Catch function allows a very short duration pulse to be qualified and lengthened to a time period long enough to guarantee that it is seen by the CPU. CPU scans necessarily vary with the length and complexity of the user's program. A scan frequency of several milliseconds is possible. On a conventional discrete input module, if a pulse is shorter than one scan time, there is a chance the CPU will not see the pulse.

The CTRIO(2) module's Pulse Catch function sees the fast incoming signal and holds its status in a status bit until the CPU can see it. A discrete output(s) can also be tied to follow the Pulse Catch.



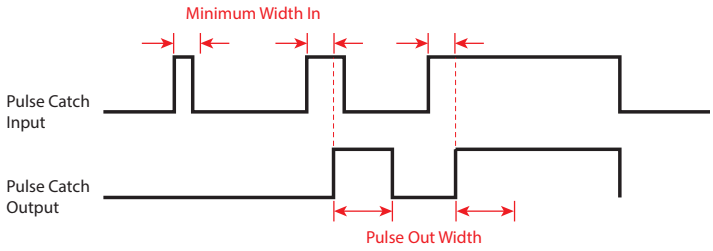
Notice that the module's four input terminals are represented by the A, B, C, and D boxes on the left side of this dialog. When wiring an input to terminal 1C, select the Channel 1 tab near the top of this window and click Pulse Catch in box C.

Three selections must be made in conjunction with the Pulse Catch option.

1. Choose the rising edge of the pulse or the falling edge of the pulse. This is a critical decision. Careful attention should be paid to the type of output the field device generates. If the signal voltage is normally low, but a short duration pulse sends the signal to the ON state, you will want to trigger off the rising edge, and vice versa.

2. Enter the minimum pulse width to capture. Transients below this width will not be recorded. Set this value by typing the desired value in the "Minimum Width In" field.

3. Enter the minimum length of pulse the CTRIO(2) module should send in response to the input pulse. Make this setting by typing in the desired value in the "Pulse Out Width" field.



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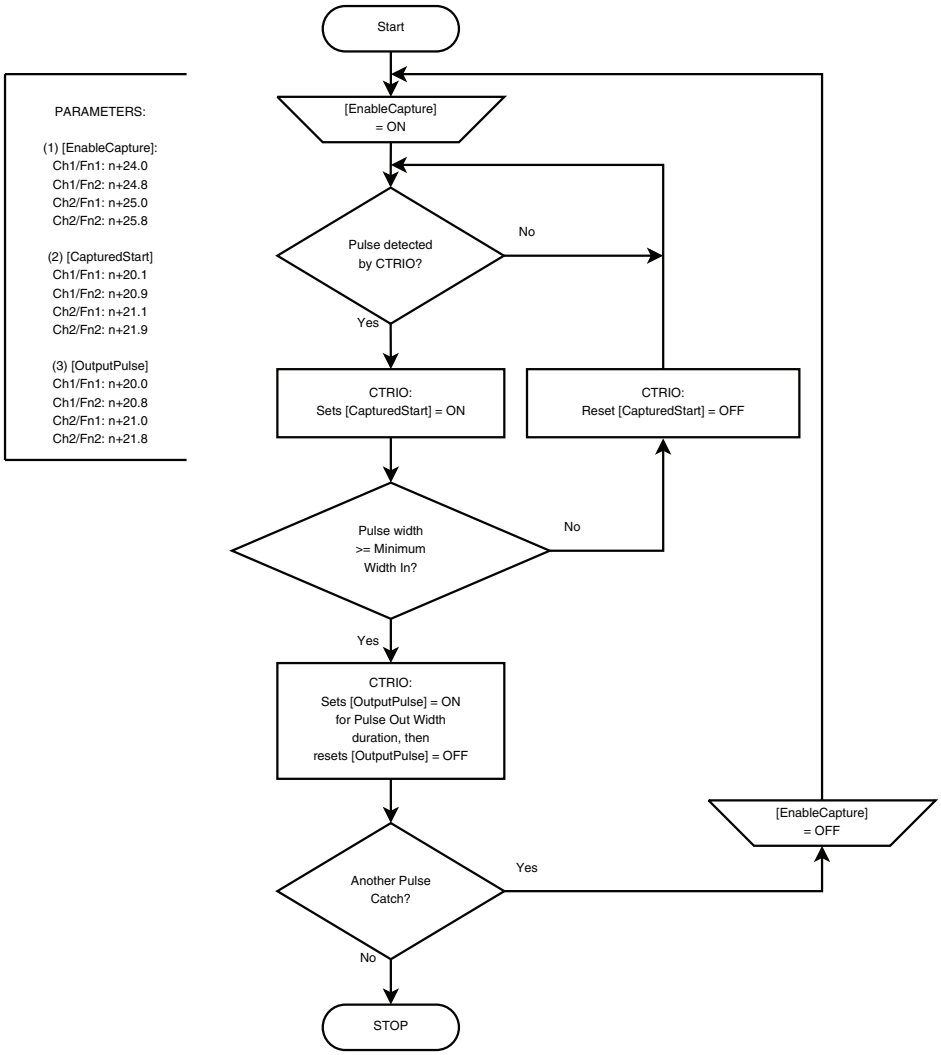
Pulse Catch Start	1, 9, 17, 25	20.1, 20.9, 21.1, 21.9

Pulse Catch Function (IBoxes & DL-PLC