3

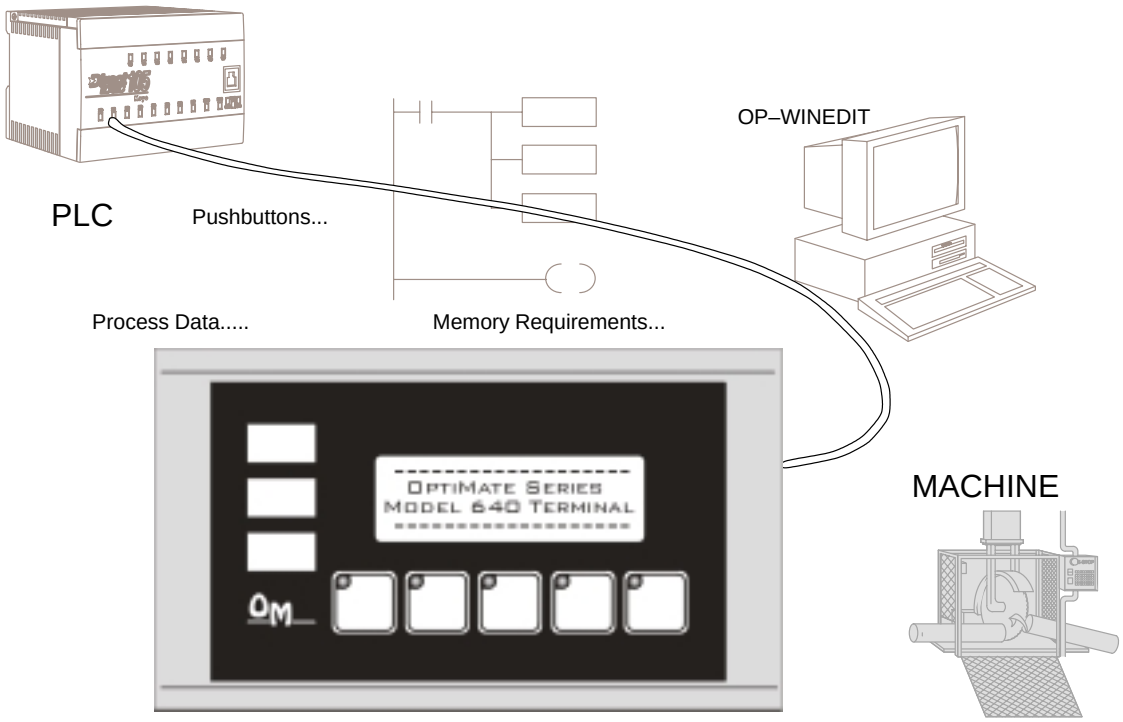
Understanding the Features

In This Chapter. . . .

Learning the Features

In this section, the subject of how to use the OP–640 features is described. The details for using pushbuttons and messages are covered. We recommend that you study this chapter before attempting to configure and use the OP-panel. As you proceed through this chapter, relate the topics discussed with how your operator panel may be implemented. The concepts discussed in this chapter are applicable to all PLCs.

- Message and Menu Operations
- Memory Mapping Process
- Controlling the Lamps
- Using the Pushbuttons
- Static Messages
- Dynamic Messages



Status and Control Registers

Status and Control Register Overview

The OP-panels communicate to the PLC through user defined PLC data registers. The starting or “Base” register is assigned during panel configuration and automatically occupies fourteen consecutive 16–bit data registers. In this manual the registers are identified as M+0, M+1, M+2, thru M+13. Each OptiMate panel which is connected to the PLC maintains separate Status and Control registers within the PLC. These registers (M+12, M+13) contain information to monitor and control individual OP-panel functions and features. Shown in the figure below, base registers M+12 and M+13 ***must have*** bit level access by the user control program. That means Status and Control **word** register memory (OP-panel Base registers) must be mapped to user memory bit registers. These bit registers are referred to as Internal Control Relays such as C0, C1, etc.

NOTE: Depending on which CPU is used and the Base memory which is assigned, the Status and Control registers *may not* require the mapping process.

Bit Level Access

Once again, the Status and Control bits are monitored and manipulated by the PLC ladder logic. For discrete operations such as pushbuttons and lamps, the registers M+12 and M+13 bits are accessed by the PLC control program. The figure below shows the fixed definition of the Status and Control register bits. These bits are labeled F1–F5 (Pushbuttons), L1–L3 (Lamps), for example. The bits and associated labels are described on the following page. First examine the figure below to begin understanding the OP-panel registers and functions. You must structure your ladder logic program to coordinate OP-panel functions asynchronously. This means the operations are triggered successively–not by a clock, but by the completion of an operation.

PLC Register	Register Function
M+0	Top line message selection
M+1	Second line message selection
M+2	Third line message selection
M+3	Bottom line message selection
M+4	Top line data
M+5	Top line data 2 (for long BCD and floating point numbers)
M+6	Second line data
M+7	Second line data 2 (for long BCD and floating point numbers)
M+8	Third line data
M+9	Third line data 2 (for long BCD and floating point numbers)
M+10	Bottom line data
M+11	Bottom line data 2 (for long BCD and floating point numbers)
M+12	Status register
M+13	Control register

MSB **Status Register M+12** **LSB**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
											F5	F4	F3	F2	F1

MSB **Control Register M+13** **LSB**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									BD	LF3	LF2	LF1	L3	L2	L1

Register Definition The following describes the function of each of the registers shown in the table.

- **Register M+0** – When a number from 1 to 160 is placed in this register, the predefined message associated with that number will be displayed on the **top** line of the LCD display.
- **Register M+1** – When a number from 1 to 160 is placed in this register, the predefined message associated with that number will be displayed on the **second** line of the LCD display.
- **Register M+2** – When a number from 1 to 160 is placed in this register, the predefined message associated with that number will be displayed on the **third** line of the LCD display.
- **Register M+3** – When a number from 1 to 160 is placed in this register, the predefined message associated with that number will be displayed on the **bottom** line of the LCD display.
- **Register M+4** – This contains numeric data associated with the **top** line display (this is described in more detail later).
- **Register M+5** – This is used for long BCD and floating point data only.
- **Register M+6** – This contains numeric data associated with the **second** line display (this is described in more detail later).
- **Register M+7** – This is used for long BCD and floating point data only.
- **Register M+8** – This contains numeric data associated with the **third** line display (this is described in more detail later).
- **Register M+9** – This is used for long BCD and floating point data only.
- **Register M+10** – This contains numeric data associated with the **bottom** line display (this is described in more detail later).
- **Register M+11** – This is used for long BCD and floating point data only.
- **Register M+12** – This is the Status Register (details below).
- **Register M+13** – This is the Control Register (details below).

Status and Control Register Definition The Status register (M+12) and Control register (M+13) are used for data exchange between the OP-panel and PLC program. The figure below shows the individual bits within each data register. The function of the Status and Control register bits are described below. Mapping these registers is covered at the end of this chapter.

MSB **Status Register M+12** **LSB**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
											F5	F4	F3	F2	F1

MSB **Control Register M13** **LSB**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									BD	LF3	LF2	LF1	L3	L2	L1

Status Register (M+12):
F1–F5 – Are the status function for the OP-panel definable pushbuttons. These bits are set to 1 (ON) when the button is active.
Control Register (M+13):
L1–L3 – Lamp ON/OFF control for each of the three lamp annunciators. Set to 1 (ON) to turn the lamp on.
LF1–LF3 – Lamp Flash control for each of the three lamp annunciators. To flash the lamp set Lamp and Lamp Flash bits both to 1 (ON).
BD– Buzzer Disable. If set to 1 buzzer does not beep when buttons are pressed.

Messages

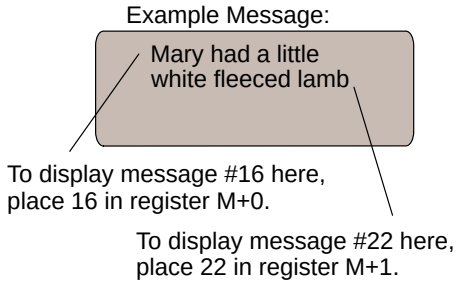
Displaying Messages on the LCD Screen

Through the OP–WINEDIT software, up to 160 predefined messages can be entered and stored in the OP–640. These messages are 20 characters long and can include a field for the display of numeric data.

Any predefined message can be displayed on either the top or bottom line. The messages entered during configuration are numbered 1 thru 160. To display a particular predefined message on the display, simply place that message's number in the message selection register.

For example, let's assume that we have defined message #16 as "Mary had a little" and message #22 as "white fleeced lamb". If we wanted to put these two lines on the top and second lines respectively, we would simply need to put the number 16 in register M+0 and 22 in register M+1.

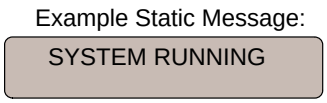
If any number other than 1 thru 160 is placed in a message selection register, the associated line will not change.



There are two types of messages which may be displayed on this panel, **Static** and **Dynamic** messages.

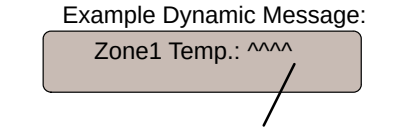
Static Messages

Static messages are text displays which have *no* embedded data. The static messages may be displayed when an event or condition becomes true. You enter the messages during configuration.



Dynamic Messages

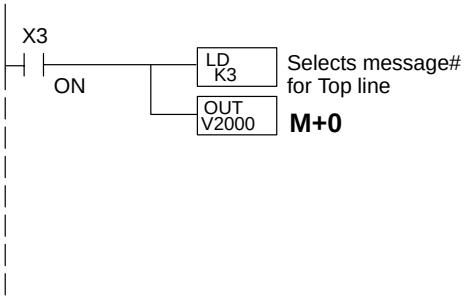
Dynamic messages are text messages which include embedded data. These messages are used to present the operator with important PLC data. This data is information which helps the operator closely monitor and control the machine or process.



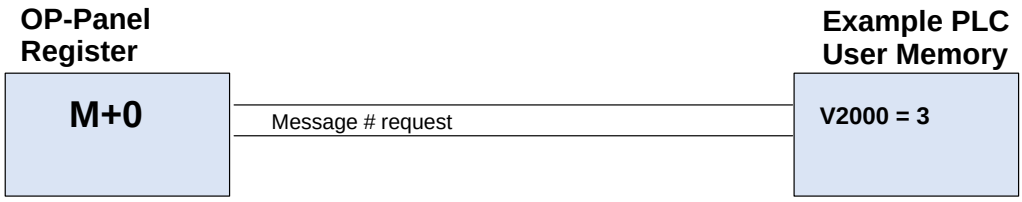
Displaying Messages

The logic required to display the configured message is quite simple. Simply put the message number (1–160) in memory location **M+0** for the top line message, **M+1** for the second line message, **M+2** for the third line message, or **M+3** for the bottom line message. The figure below demonstrates an example of a Static message with the panel configured for a starting address of V2000.

Static Message Operation



In this example, if the PLC's input signal X3 is ON, the 16 bit integer (K3) value is placed in Word register V2000 (M+0), selecting message #3 to be displayed on the top line.



Static Display

Description

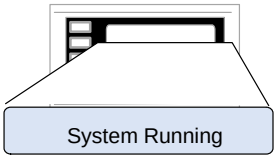
All supported CPUs use the first OP-panel register for displaying a top line static message.

Your ladder logic program must sequence the message being displayed by placing an integer value (1–160) in register M+0.
The OP-panel operating system automatically updates the latest messages according to values placed in the highlighted registers.

Top Line Static Message

Register	Value	Function
M+0	**3**	Top line message selection
M+1		Second line message selection
M+2		Third line message selection
M+3		Bottom line message selection
M+4		Top line data
M+5		Top line data 2
M+6		Second line data

Example Message #3



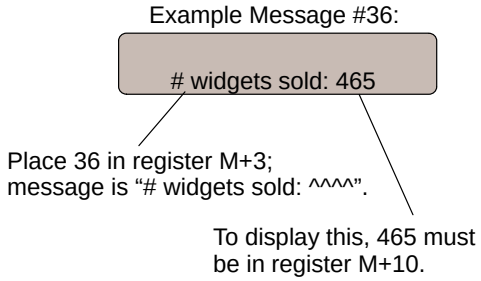
Dynamic Message Operation

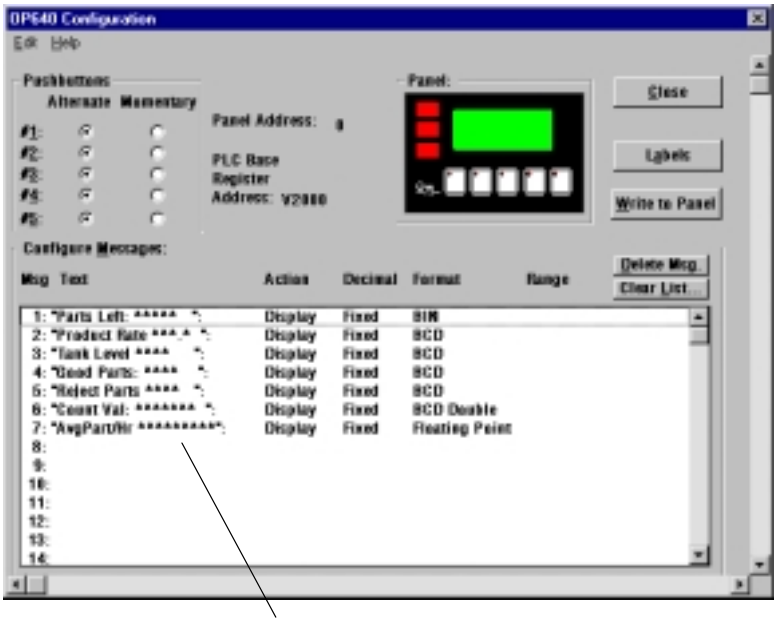
You may program message numbers 1–160 to be used as dynamic messages. One numeric field per line is allowed. Dynamic messages may be displayed on either the top or bottom display lines. The maximum number of digits which may be displayed is five if binary data format is used, four if BCD is used, and eight if BCD double is used. The figure below demonstrates the OP–WINEDIT screens for programming a dynamic message.

Enter the message text and place the caret (^) symbol(s) depending on the number of digits you would like to display. The value range which may be displayed is 0–65,535 integer, 0–9999 BCD or 0–99999999 BCDD. Choose binary, BCD, or BCD double format and fixed point decimal placement.

For dynamic messages which require fixed decimal point placement within the value, you must use the OP–WINEDIT to perform parameter placement type. For fixed position decimal points you must enter the decimal directly into the message text, such as Zone1 Temp = ^^.^^.

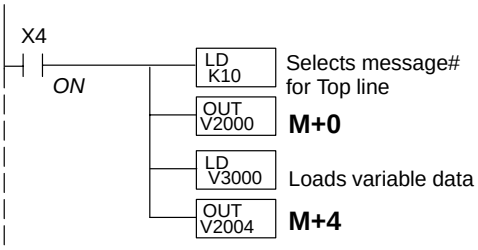
For example, let's say message #36 is "# widgets sold: ^^^^". Let's also say that 465 widgets have been sold today. To display the current number of widgets sold on the bottom line of the display, you would place 36 in register M+3 and 465 in register M+10. The bottom line would then display: "# widgets sold: 465".



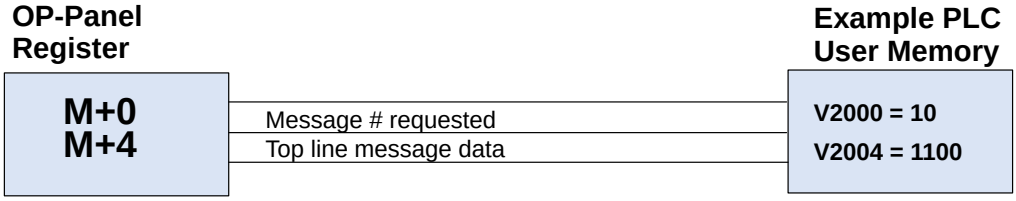


Examples of dynamic messages. Notice the caret (^) symbols, which is where data will be when the message is displayed.

Dynamic Message Top Line

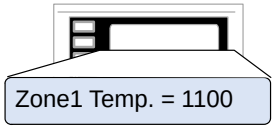


In this example, if the PLC's input signal X4 is ON, the 16 bit integer (K10) value is placed in Word register V2000 (M+0) selecting message #10 to be displayed on the top line. The data value in register V3000 (let's say 1100) is moved into V2004 (M+4), which is embedded in the top line message. The top line data value will update as long as X4 is enabled (ON).



Remember, your ladder logic program must select the message being displayed by placing an integer value between 1 and 160 (message #) in register M+0. The embedded data for the top line message is controlled by loading a 16 bit value into register M+4.

Example Message #5

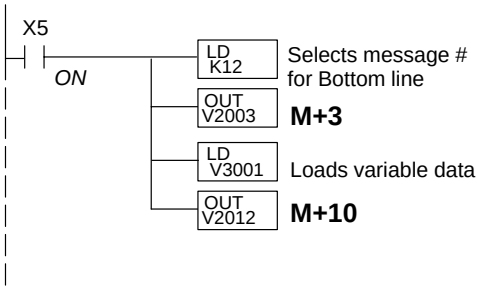


Top Line Dynamic Message

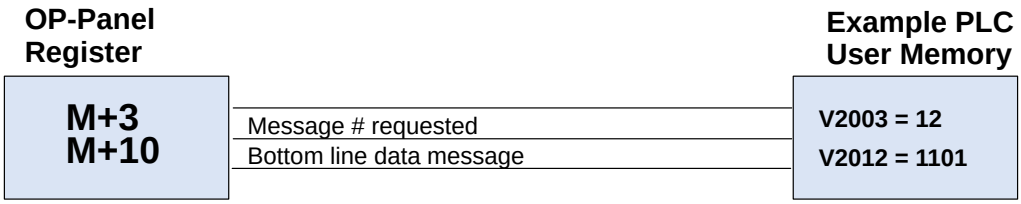
Register	Value	Function
M+0	**10**	Top line message selection
M+1		Second line message selection
M+2		Third line message selection
M+3		Bottom line message selection
M+4	**1100**	Top line data
M+5		Top line data 2
M+6		Second line data

The highlighted registers M+0 and M+4 in this figure result in displaying this top-line dynamic message.

Dynamic Message Bottom Line

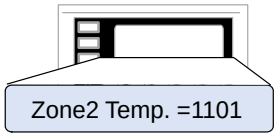


In this example, if the PLC's X5 input signal is ON, the 16 bit integer (K12) value is placed in Word register V2003 (M+3) requesting message #12 to be displayed on the bottom line. The data value in register V3001 (let's say 1101) is moved into V2012 (M+10), which is embedded in the bottom line message. The bottom line data value will update as long as X5 is enabled (ON).



Remember, your ladder logic program must select the bottom line message being displayed by placing an integer value between 1 and 160 (message #) in register M+3.

Example Message #12



Bottom Line Dynamic Message

Register	Value	Function
M+0		Top line message selection
M+1		Second line message selection
M+2		Third line message selection
M+3	**12**	Bottom line message selection
⋮	⋮	⋮
M+10	**1100**	Bottom line data

The highlighted registers shown in this figure results in displaying this bottom-line dynamic message.

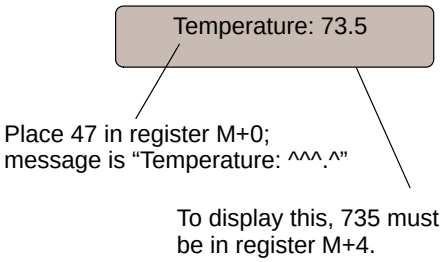
Displaying Data With a Decimal Point

The OP–640 panel allows you to display fixed point numbers, which are numeric values that have a known decimal point placement and are simply handled as integer values within the PLC program. The only time you see an actual decimal point is on the LCD display. An example of a fixed point number is a program that uses temperature as a control variable, and within the program all temperatures are scaled in tenths of a degree. The values are integer, so a temperature of 73.5 degrees would be 735 in a data register. For the convenience of the operator, you would want the LCD display to include the decimal.

Fixed point numbers are handled by simply placing a decimal point or period in the message field during configuration.

For example, let's say you want to display the message "Temperature: 73.5" on the top line, and the message is #47. Enter message #47 as "Temperature:^^^.^" during configuration.

Example Message #47:

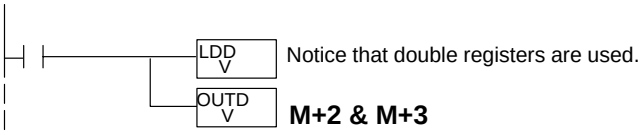


Displaying BCD and Binary Numbers

Normally, numeric values to be displayed are values contained in one 16-bit register. One 16-bit register will handle values between 0 and 65535 in binary form, or between 0 and 9999 in BCD form. For these type numbers register M+4 is used for the numeric value for the top line, M+6 is used for the second line, M+8 is used for the third line, and M+10 is used for the bottom line.

Displaying BCD Double Numbers

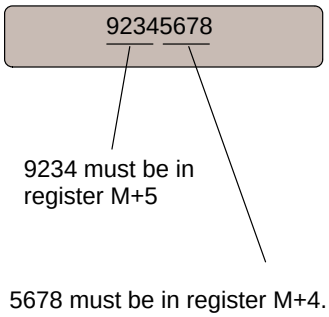
The OP–640 will handle large numeric numbers. If you select the option **BCD Double** when the display message is being defined, your display can handle numbers between 0 and 99,999,999. The panel will use data in the register pair M+4 and M+5 for the top line, and use M+6 and M+7 for the second line, etc. The data must be in BCD.



When placing a BCD double number in the display registers, the first register numerically in the sequence of two registers (M+4, M+6, M+8 or M+10) will contain the *four least significant digits* of the number. The second register in the sequence (M+5, M+7, M+9 or M+11) contains the data for the *four most significant digits* of the BCD double number.

For example, to display the number 92345678 on the top line of the display, the top line data registers, M+4 and M+5, must contain 5678 and 9234 respectively.

Example: BCD Double



Displaying Floating Point Numbers

The OP–640 has the capability to display Floating Point (or Real) numbers if you select the option **Float** when the display message is being defined in the OP–WINEDIT software.

Floating point numbers can only be used with the D2–250, D3–350, and D4–450 CPUs since they are the only compatible CPUs that support the IEEE 32-bit floating point number format, which is where the floating point numbers are stored. They always occupy two 16-bit register locations regardless of the size of the number. See the PLC User Manual for more information on the IEEE 32-bit floating point number format.

An IEEE 32-bit floating point number has a range of –3.402823E+38 to +3.402823E+38. The OP–640 will be able to display any number within that range. The panel always uses the format ±X.XXE±XX to display the numbers.

The panel does not have the ability to display all the significant digits of a floating point number, it only displays the first three significant digits. The OP–640 truncates the remaining digits so you always see the true number. The two examples below show the data contained in the PLC registers and the corresponding value displayed on the panel in its format. Notice how the data is truncated, not rounded.

The configuration of a floating point number message is similar to any other message. First, you select the message number, then type in the text using nine caret symbols (^) as a place holder for each of the nine floating point number symbols. To do this, type in one caret symbol, select the **Float** option for the data format, and then type in the remaining eight caret symbols.

Example: Floating Point Numbers

PLC Registers	OP–640 Display
12301.789	+1.23E+04
123.96783	+1.23E+02

For example, let's say you wanted to configure message #58 to display a floating point number. In the OP–WINEDIT software, select OP–640 as the module type, and then select message #58 with the mouse. Type in the following message: "Float Pt ^^^^^^^^^" and select floating point as the message format (you must type in at least one caret symbol and then select Float before you can type in all nine caret symbols).

To display a number, simply move it into either the top or bottom line data registers and load the appropriate message number into the corresponding top or bottom line message selection register. For example, if you display the number 632.15 in message #58, it will be displayed as "Float Pt # +6.32E+02".

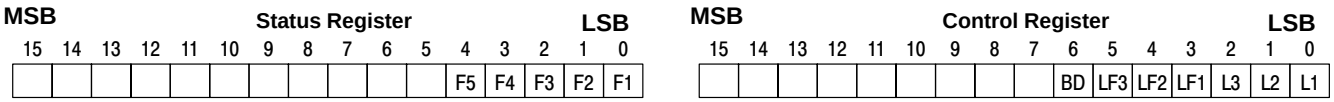
Pushbuttons and Lamps

The OP–640 has five user-defined pushbuttons. Pushbuttons may be used to begin events or tasks within the PLC, such as start/stop control. This section describes concepts of how to monitor and control the pushbuttons on your OP-panel.

Pushbutton Operation

The OP-panel pushbutton inputs are monitored for ON/OFF conditions in your PLC ladder logic program. From a practical point of view we need to control and monitor the bits in the status register on an individual basis. The OP–640 pushbuttons are assigned to the *first five bits* of the **Status Register (M+12)**. Examine the highlighted status bits below which show each user-definable pushbutton.

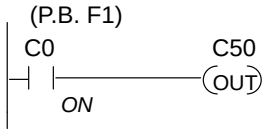
M+10	Bottom line data
M+11	Bottom line data 2 (for long BCD and floating point numbers)
M+12	Status register
M+13	Control register



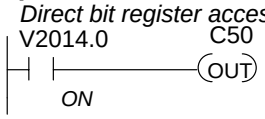
Pushbutton Example

The pushbutton example shown here is using ***Direct***LOGIC PLC address references. The equivalent instructions for *other* PLC products supported are shown in Chapter 5 of this manual.

NOTE: In this example we assume that the OP-panel is configured with a base register of V2000. In this case, status register M+12 is V2014 which we will assume has been mapped to V40600, the ***Direct***Logic internal control relay memory**.** Mapping details are discussed later in this chapter.

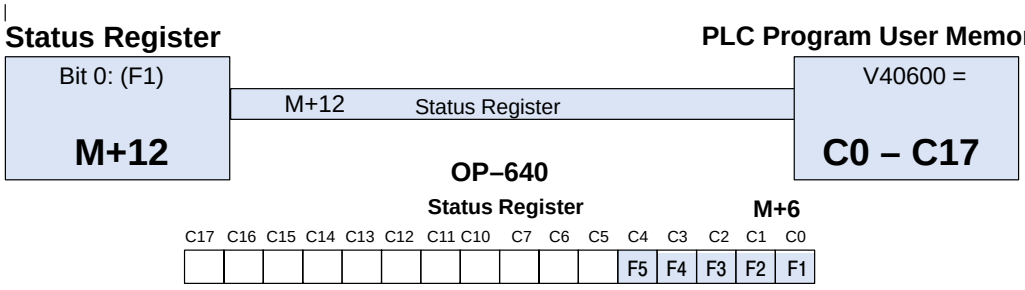


(D2–250/D3–350/D4–450 Only)
Direct bit register access



In this example, C0 represents the pushbutton No.1 (F1) via the mapping process. When push-button No.1 is pressed C0 is true and Coil C50 is energized.

Status Register (M+12) = V40600: C0 – C17



Pushbuttons Using Direct Access to Status Register Bits

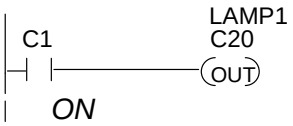
The ***Direct***Logic D2–250/D3–350/D4–450 CPUs and the Allen-Bradley SLC 5/03 and 5/04 support instructions which provide individual status bits access. This is called **Bit-of-Word** capability. For example, in the previous example, the ladder logic for the D2–250/D3–350/D4–450 monitors the first bit of the status word directly. Once again, our example assumes that we configured the OP-panel with a starting base address of V2000.

Pushbutton LEDs

There are LEDs located on each of the user defined pushbuttons, indicating pushbutton status (ON or OFF). You may choose the pushbutton type (alternate or momentary) while configuring your OP-panel. In the case of an alternating configured pushbutton, the LED will change state each time the pushbutton is pressed. With momentary configured pushbuttons the LED is ON only as long as the pushbutton is being pressed.

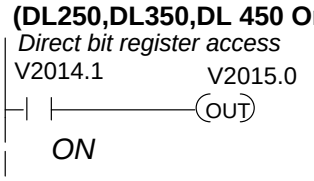
Lamp Example

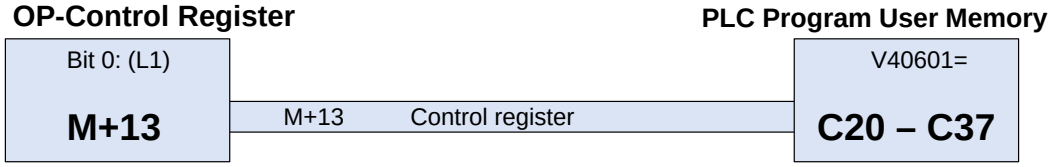
The lamp examples shown here are using ***Direct***LOGIC PLC address references. The equivalent instructions for *other* PLC products supported are shown in Chaper 5.



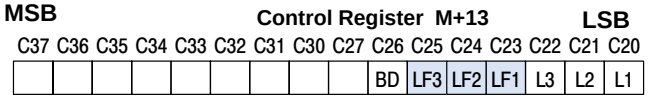
In this example, C1 represents the pushbutton No.2 (F2) via the mapping process. When *alternating* pushbutton No.2 is pressed internal Control Relay C20 is true and via mapping process Control register Bit 0 (L1 Lamp) is energized.
* Control Register (M+13) = V40601: C20 – C37

(DL250,DL350,DL 450 Only)



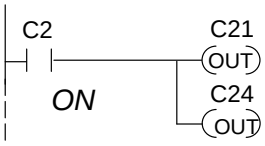


All lamps may be controlled using the concept shown above. You may use the Lamp Flash option by controlling the appropriate Flash bit via the ladder logic program. The example figure below demonstrates how to use the Control register Flash bits (LF1, LF2, and LF3).



Lamp Flash

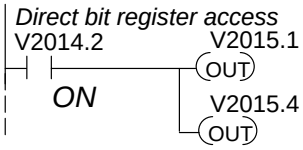
The lamp flash examples shown here are using ***Direct***LOGIC PLC address references. The equivalent instructions for *other* PLC products supported are shown in Chapter 5.



In this example, C2 represents the pushbutton No.3 (F3) via the mapping process. When *alternating* pushbutton No.3 is pressed internal Control Relay C21 and C24 are energized ON. This process manipulates Control register bit 1 and bit 4 which controls yellow lamp and flashing.

*Control Register (M+13) = V40601: C20–C37

(DL250/D3–350/D4–450 Only)



Memory Mapping Process

Each OP–640 is assigned 224 bits of PLC user memory which will be used as the OP-panel database. The ladder logic program must access this assigned OP-panel memory. Let's take a closer look at this user memory and how it relates to the OP-panel features.

OP Base Register Memory Definition

As discussed earlier, regardless of which PLC product you are using the base registers addressed M+0 through M+13 are formatted the same. In this manual, when the terms M+0 through M+13 are used, this identifies which base register(s) are affected for the topic being covered.

Operator Panel Base Memory

PLC user memory is assigned to each panel with the OP–WINEDIT configuration software. For new OP-panels and add-on applications the programmer must define fourteen 16-bit registers for PLC interface. Below is a figure showing memory layout for ***Direct***LOGIC DL05, DL105, DL205, D3–350, DL405 PLC's and uses V2000–V2015 for the OP–640 panel. See the next page for other PLC product memory usage examples.

You must reserve 224 bits (fourteen 16-bit registers or twenty-eight 8-bit registers) which are used to process data between the panel and your PLC. You must configure the **Base** register for the OP-panel. This base register address is stored in the OP-panel memory.

CPU User's memory

	OP–640 Panel Data Base	
V2000	M+0	16 bits
V2001	M+1	16 bits
V2002	M+2	16 bits
V2003	M+3	16 bits
V2004	M+4	16 bits
V2005	M+5	16 bits
V2006	M+6	16 bits
V2007	M+7	16 bits
V2010	M+8	16 bits
V2011	M+9	16 bits
V2012	M+10	16 bits
V2013	M+11	16 bits
V2014	M+12	16 bits
V2015	M+13	16 bits
	Total: 224 bits	

OP-Panel User Memory

Let's examine the different address conventions for ***Direct***LOGIC and Allen-Bradley. For example, the ***Direct***LOGIC address references are **octal**, and the Allen-Bradley is **decimal**.

The ***Direct***LOGIC DL05/DL105/DL205/D3–350/DL405 OP-panel address uses V-memory registers which are 16-bit registers. The D3–330/340 CPUs use reference assignments with 8-bit registers. This means that they require fourteen 8-bit registers for data handling. The Allen-Bradley memory is defined with a reference **(Nx)** which represents the memory area, and **(:n)** which defines the word within the memory area. Please refer to the appropriate CPU User manual for the PLC product you are using.

DirectLOGIC PLCs

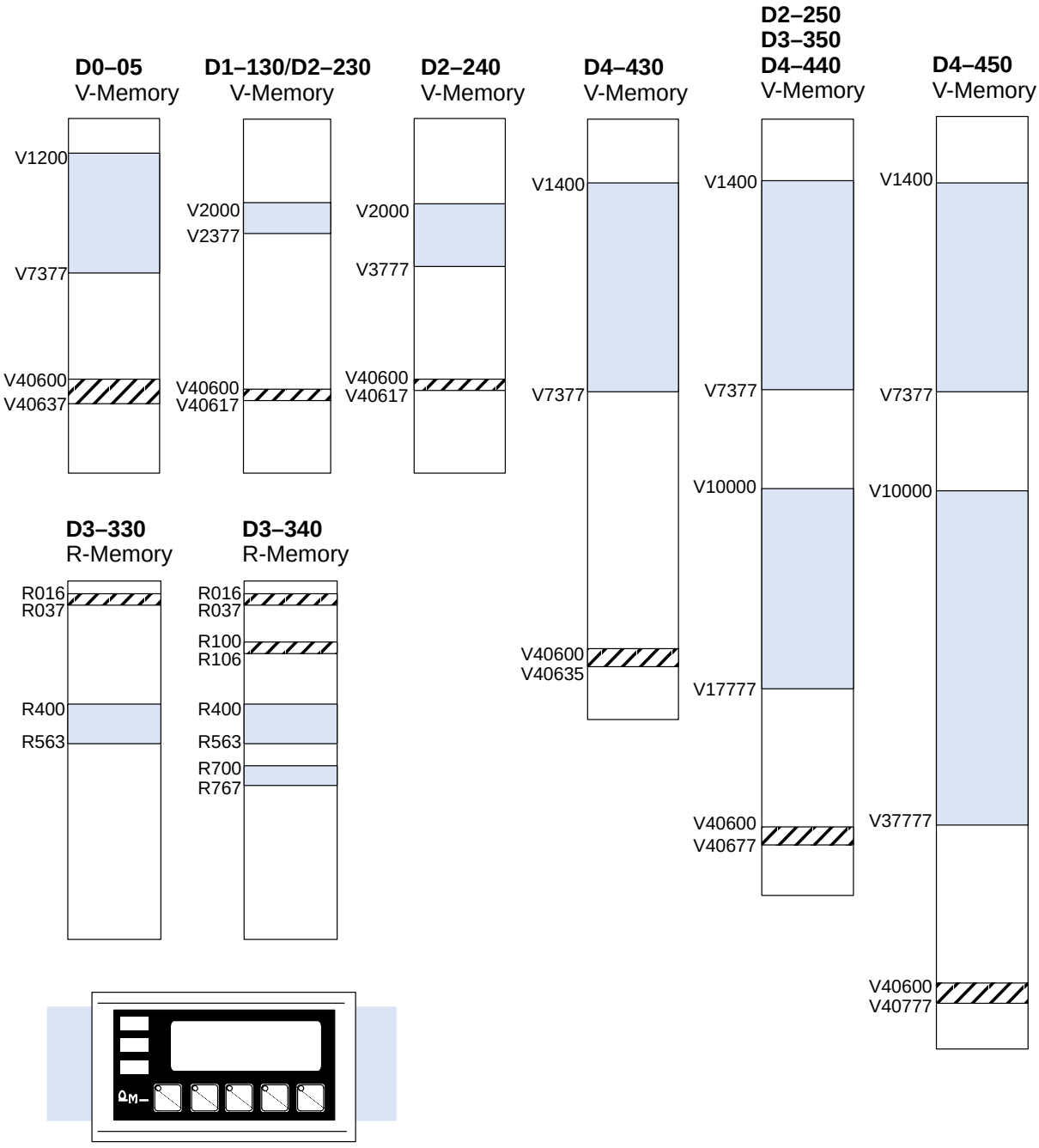
Example PLC Register Address			Register Function
DL05/105/205/ D3–350/DL405	D3–330/ D3–340	Generic	
V2000	R400/R401	M+0	Top line message selection
V2001	R402/R403	M+1	Second line message selection
V2002	R404/R405	M+2	Third line message selection
V2003	R406/R407	M+3	Bottom line message selection
V2004	R410/R411	M+4	Top line data
V2005	R412/R413	M+5	Top line data 2 (for long BCD and floating point numbers)
V2006	R414/R415	M+6	Second line data
V2007	R416/R417	M+7	Second line data 2 (for long BCD and floating point numbers)
V2010	R420/R421	M+8	Third line data
V2011	R422/R423	M+9	Third line data 2 (for long BCD and floating point numbers)
V2012	R424/R425	M+10	Bottom line data
V2013	R426/R427	M+11	Bottom line data 2 (for long BCD and floating point numbers)
V2014	R430/R431	M+12	Status register
V2015	R432/R433	M+13	Control register

Allen-Bradley SLC 500

Example PLC Register Address		Register Function
N7:0	M+0	Top line message selection
N7:1	M+1	Second line message selection
N7:2	M+2	Third line message selection
N7:3	M+3	Bottom line message selection
N7:4	M+4	Top line data
N7:5	M+5	Not used (see Note)
N7:6	M+6	Second line data
N7:7	M+7	Not used (see Note)
N7:8	M+8	Third line data
N7:9	M+9	Not used (see Note)
N7:10	M+10	Bottom line data
N7:11	M+11	Not used (see Note)
N7:12	M+12	Status register
N7:13	M+13	Control register

NOTE: While the OP–640 will display BCD Double and Floating Point numbers, it does not support these functions when used with Allen–Bradley PLCs.

*Direct*LOGIC **User Memory Overview**



User Data Space available for OP-panels

Internal Relay Memory

DirectLOGIC PLCs use octal addressing, as indicated by the shaded areas.

Mapping Operation

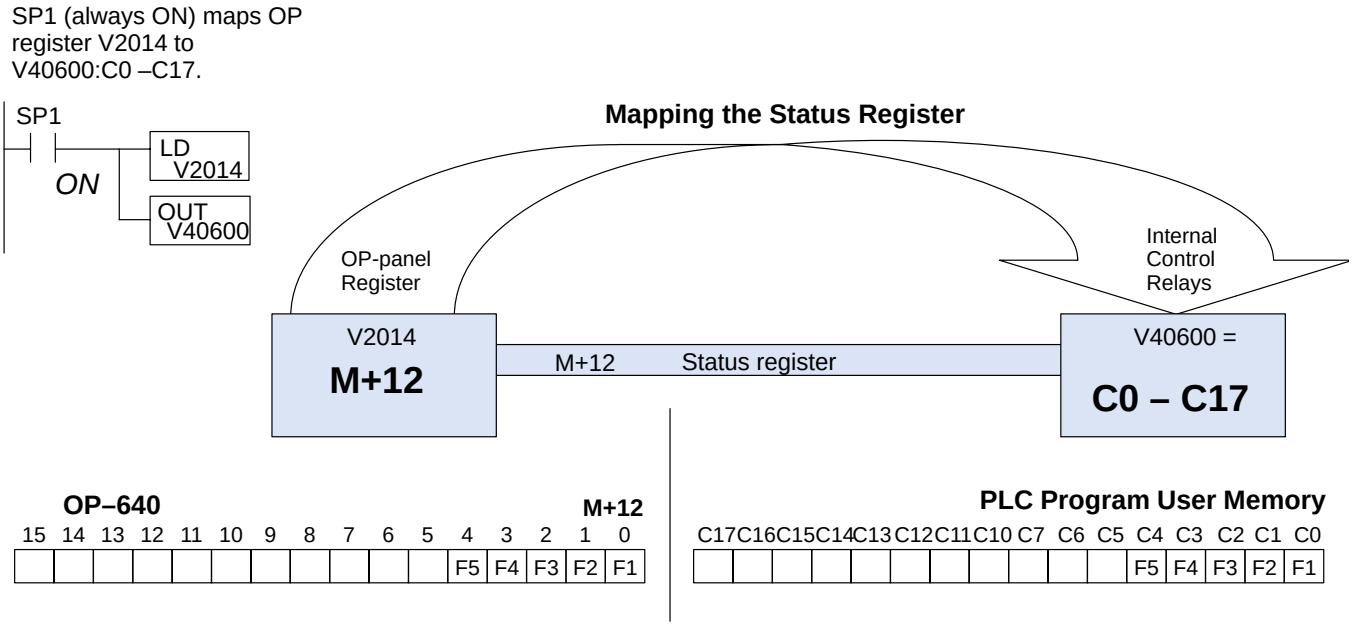
We explained earlier that the PLC and OP-panel must exchange data on a *bit-level* basis. For ***Direct***LOGIC controllers, the OP-panel Status Register (M+12) must be mapped into internal control relays such as C0, C1, etc (and the control relays C20–C37 must be mapped into the Control Register, M+13). This allows *direct access* to the Status bit register and the Control bit register. You must execute mapping every CPU scan in order to update data between the OP-panel and PLC.

The following examples assume the OP-panel starting base-register (M+0) is assigned to word register V2000. For example, the DL05, DL105, DL205, D3–350, and DL405 CPUs have internal control relays starting at register V40600. They are designated as C0, C1, etc. Mapping updates status data (M+12) into base register V2014 and control data (M+13) into base regiser V2015 with each PLC scan.

Mapping Examples (DL05, 105, DL205, D3–350, and DL405)

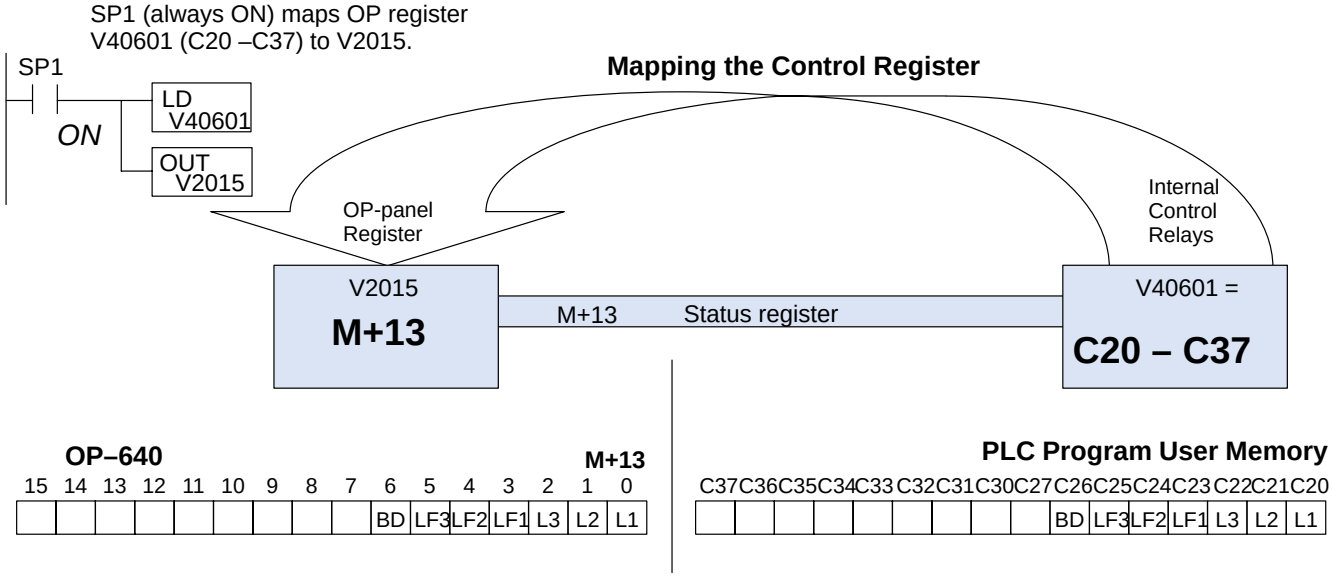
Mapping the Status Register

The figure below demonstrates how the OP-panel status register is mapped to user memory for bit manipulation. Notice the sixteen bits in the status register are loaded into the Internal Control Relays C0–C17. These control relays are used within the ladder logic program for monitoring pushbuttons and coordinating data entry control.



Mapping the Control Register

The figure below demonstrates how the Internal Control Relays C20–C37 are mapped to the OP-panel control register. Notice the sixteen bits in the Internal Control Relays C20–C37 are loaded into the control register. These control relays function as outputs for the Lights.

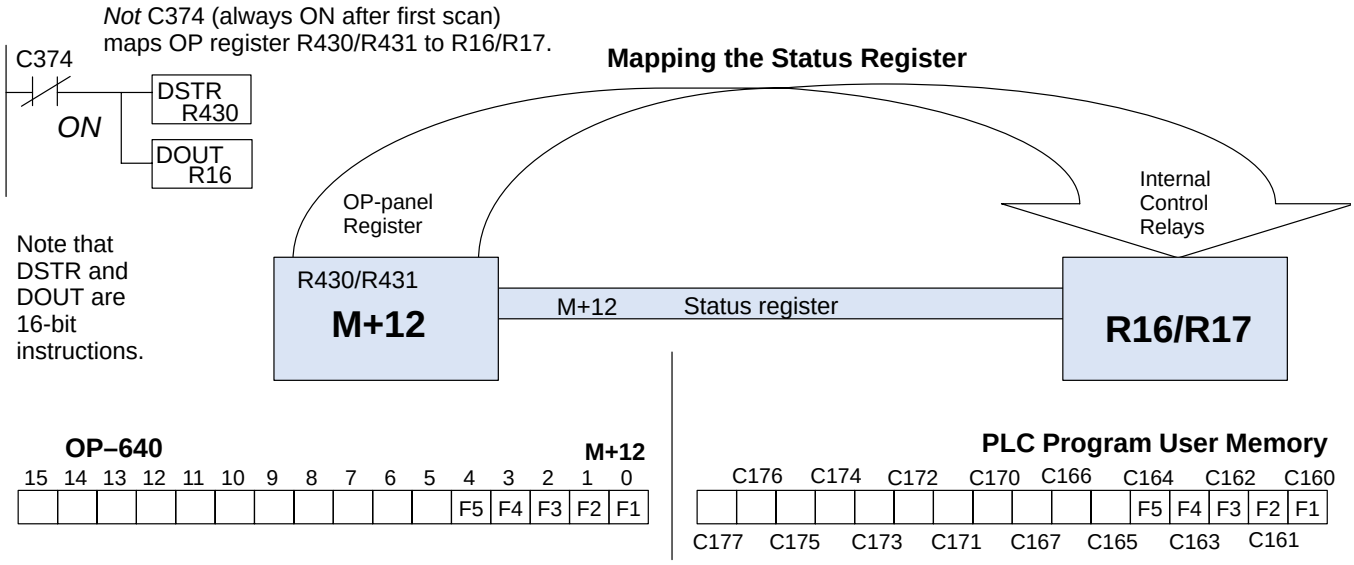


Mapping Example (D3–330/340)

Unlike the DL05, DL105, DL205, D3–350, and DL405 mapping examples, the D3–330/340 CPUs use 8-bit words. So it takes two 8-bit words for each mapped memory location because each mapped memory location needs sixteen consecutive bits. We will assume that R400 was used as the base register address and we want the mapping to start at R16 for the status register.

Mapping the Status Register

The figure below demonstrates how the OP-panel status register is mapped to user memory for bit manipulation. Notice the sixteen bits in the status register are loaded into the Internal Control Relays C160–C177. These control relays monitor pushbuttons and coordinate data entry control.



Mapping the Control Register

The figure below demonstrates how the Internal Control Relays are mapped to the OP-panel control register. Notice the sixteen bits in the Internal Control Relays C200–C217 are loaded into the control register. These control relays function as outputs for the Lights.